**NIRMA UNIVERSITY**

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| **Institute:** | Institute of Technology |
| **Name of Programme:** | Integrated B.Tech.(CSE)-MBA |
| **Course Code:** | CSI0501 |
| **Course Title:** | Computer Architecture |
| **Course Type:** | Core |
| **Year of Introduction:** | 2021-22 |

**Credit Scheme**

| L | T | Practical Component | | | | C |
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**Course Learning Outcomes (CLO):**

At the end of the course, students will be able to –

1. illustrate the basics of various architectural units of the Computer System
2. apply the knowledge of combinational and sequential logical circuits to mimic a simple computer architecture
3. demonstrate the simulations for basic computer operations
4. appraise the importance of parallelism in computer architecture

**Syllabus:** **Total Teaching hours: 30**

| Unit | Syllabus | Teaching hours |
|---|---|---|
| Unit-I | **Introduction to Computer Architecture Register transfer and Micro operations:** Register transfer language -Register transfer, Bus and memory transfer, Arithmetic micro-operations, Logic Micro operations, Shift micro-operations and Arithmetic logic shift unit. **Instruction codes:** Computer registers, Computer instructions, Timing and control, Instruction cycle, Memory reference instructions, Input-Output and interrupt, complete computer description. | 08 |
| Unit-II | **Micro programmed Control:** Control Memory, Address sequencing, Microprogram example, Design of Control unit **Central Processing Unit:** Introduction, General register organization, Stack organization, Instruction formats, Addressing modes, Data transfer and manipulation, Program control, Reduced instruction set computer (RISC). Complex Instruction Set Computer (CISC), Comparison of RISC and CISC Parallel Processing, Pipelining, Arithmetic pipelining, Instruction pipelining, RISC pipeline, vector processing, Array processors | 08 |
| Unit-III | **Computer Arithmetic:** Binary Arithmetic's, Add, Subtract, Multiply Divide, Algorithms, and Implementations Carry Look Ahead and Fast Adders. | 05 |
| Unit-IV | **Input Output Organization:** Input output interface, Asynchronous data transfer, Modes of transfer, Priority interrupt, Direct Memory access (DMA), Input output processor (IOP), CPU-IOP communication, Serial communication. | 05 |
| Unit-V | **Memory Organization:** Memory hierarchy, Main memory, Auxiliary memory, Flash memory, Associative memory, Cache memory, Virtual | 04 |

memory.

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| Self-Study: | The self-study contents will be declared at the commencement of semester. Around 10% of the questions will be asked from self-study contents |
| Suggested Readings/ References: | 1. M. Morris Mano, Computer System Architecture, Prentice Hall of India<br>2. Williams Stallings, Computer Organization and Architecture Prentice Hall of India<br>3. Douglas V Hall Microprocessors and Interfacing Programming and Hardware, Tata McGraw Hill<br>4. V. Carl Hamacher, Zvonko G. Vranesic and Safwat G. Zaky, Computer Organization, Mcgraw Hills Publisher<br>5. M. Radhakrishnan, D. Balasubramanian, Computer Installation and Troubleshooting, ISTE Learning Materials |
| Suggested List of Experiments: | -NA- |
| Suggested Case List: | -NA- |