NIRMA UNIVERSITY
SCHOOL OF TECHNOLOGY, INSTITUTE OF TECHNOLOGY
M. Tech. in Electronics and Communication Engineering (Embedded System)
M.Tech. Semester - II

Department Elective I

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Course Code	**3EC32D102**
Course Title	**Design of Integrated Circuits**

Course Outcomes (COs):

At the end of the course, students will be able to -

1. Analyse MOS based circuits working under linear and saturation region of operation.
2. Evaluate performance of MOS based analog and digital integrated circuit applications.
3. Design and optimize CMOS based digital combinational and sequential circuits for given specifications.
4. Design single stage amplifier and current mirror circuits using MOS.

Syllabus: **Teaching Hours:**

UNIT I: Introduction to VLSI **02**

Introduction, Design methodology, Level of abstractions, Design flow, Design approaches, Design styles, Design considerations, Design quality-reliability- updateability, EDA tools

UNIT II: MOS Transistor **10**

The Metal Oxide Semiconductor (MOS) structure, The MOS system under external bias, Structure of MOS transistor, Operation of MOS transistor, MOSFET Current-Voltage characteristics, MOSFET scaling and small-geometry effects, MOSFET capacitances, MOS modelling, CMOS processing, Fabrication Process flow - basic steps, C-MOS n-Well Process, Layout design rules, and Full custom mask layout design

UNIT III: MOS Small Signal and Large Signal Analysis **12**

Introduction, Resistive load inverter, Inverter with n-type MOSFET load (Enhancement type MOSFET load), Inverter with n-type MOSFET load (Depletion type MOSFET load), CMOS inverter and its analysis, Noise margin, Circuit power consumption, Capacitance estimation, Speed-power-area trade-off, Buffer design,

UNIT IV : MOS Switching Characteristics **06**

MOS inverters Switching characteristics and Interconnect effects, Delay-time definitions, Calculation of delay time, Switching power dissipation of CMOS Inverters

UNIT V: Combinational and Sequential MOS Logic Circuit **10**

NOR2 Gate, NAND2 Gate, Layout and design rules, Stick Diagram, From transistor level schematic to Layout, Layout of simple CMOS Logic Gate, Complex Logic Circuits, Transistor level Schematic of Complex Logic Circuits, Significance of Euler path, pseudo NMOS realization, CMOS transmission gates, Complementary Pass transistor Logic, Latch and Flip-flop circuit, Dynamic logics

UNIT VI: CMOS Analog Circuit Design **05**

Current Mirrors and Single Stage Amplifiers

Self-Study:

The self-study contents will be declared at the commencement of semester. Around 10% of the questions will be asked from self-study contents.

Suggested Readings:

1. S. M. Kang ,Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, McGraw Hill.
2. David A Johns, Ken Martin, Analog Integrated Circuit Design, John Wiley and Sons Inc.
3. B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw- Hill.
4. Philip E. Allen, Douglas R.Holberg, CMOS Analog Circuit Design, Oxford University Press.

L = Lecture, T = Tutorial, P = Practical, C = Credit