NIRMA UNIVERSITY
SCHOOL OF TECHNOLOGY, INSTITUTE OF TECHNOLOGY
B.Tech. Electronics & Communication Engineering
Semester - VI

L	T	P	C
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Course Code	**2EC601**
Course Title	**Computer Architecture**

Course Outcomes (COs):
At the end of the course, the students will be able to
1. Evaluate the performance of the processor for given specifications.
2. Design arithmetic logic unit for a given instruction set.
3. Analyse the performance of a single and multicycle data path.
4. Realize cache mapping and virtual memory address translation schemes.

Syllabus: **Teaching Hours:45**

UNIT 1: Computer Performance **04**
Cost and Performance, Performance enhancement, Amdahl's law, Performance estimation.

UNIT II: Instruction Set Architecture of MIPS Processor **06**
Instructions format, Addressing modes, Procedure and Data, Assembly language programming, Instruction set variation.

UNIT III: Arithmetic and Logical Unit Design **06**
Design of Adders and simple ALU, Multiplier and Divider.

UNIT IV: Data Path and Control Path of MIPS processor **15**
Instruction execution steps, single cycle and Multi-cycle data path, Performance of single and multi-cycle data path, Control unit synthesis, Microprogramming, Pipe-lined data path, pipeline performance limits, Data dependencies and Hazards, branch prediction algorithms.

UNIT V: Buses, Links and Interfacing **08**
Intra and Intersystem links, types of buses and its characteristics, bus communication protocols, bus arbitration and performance, basics of interfacing and interfacing standards.

UNIT VI: Memory Organization **06**
Memory hierarchy, SRAM, DRAM, Cache organization, Cache mapping schemes, Improving cache performance, Virtual Memory, Address translation, Translation look aside buffer.

Self-Study:
The self-study content will be declared at the commencement of the semester. Around 10% of the questions will be asked from self-study content.

Laboratory Work:
Laboratory work will be based on the above syllabus with a minimum of 10 experiments to be incorporated.

Suggested Readings:

1. Behrooz Parahami, Computer Architecture from Microprocessor to Super Computer, Oxford University Press
2. J. Hayes, Computer Architecture and Organization, TMH
3. Govind Rajalu, Computer Architecture, TMH
4. D. Patterson and J. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Morgan Kaufman

L = Lecture, T = Tutorial, P = Practical, C = Credit