NIRMA UNIVERSITY
SCHOOL OF TECHNOLOGY, INSTITUTE OF TECHNOLOGY
B.Tech. Electronics & Communication Engineering
Semester - VI
Department Elective III

L	T	P	C
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Course Code	2ECDE59
Course Title	Testing and Verification of Digital Circuits

Course Outcomes (COs):
At the end of the course, the students will be able to
1. Perform functional and timing verification.
2. Identify possible physical defects and model them as logical faults to determine their concerned test vectors.
3. Develop scan chain insertion and generate the test set.
4. Develop Design-for-Test and Built-In-Self-Test circuits as per the given applications.

Syllabus: **Teaching Hours:45**

UNIT I: Introduction to Testing **04**
Testing philosophy, Role of testing, Digital and analog circuit testing, Technology trends affecting testing.

UNIT II: Test Equipment, Economics and Quality **02**
Test economics, Defining cost, Benefit-cost analysis, The rule of ten, Yield.

UNIT III: Verification **06**
Importance of verification, Verification plan, Verification flow, Levels of verification, Verification methods and languages, Functional Verification: Introduction to testing bench, Testbench architecture, Types of test benches, Case study.

UNIT IV: Static Timing Analysis **05**
Need for Timing Analysis, Dynamic Timing Analysis, Static Timing Analysis, Critical Path and Maximum Operating Frequency, Set-up and Hold Time Violation, Remedies for Violation, Time Borrowing.

UNIT V: Fault Modelling **07**
Defects- Errors-Faults, Functional Versus Structural Testing, Level of fault models, A glossary of fault models, Single stuck-at fault, Multiple stuck-at faults, Fault equivalence.

UNIT VI: Design For Testability **07**
Ad-hoc Design for Testability techniques, Structured DFT, Scan-Chain insertion, Scan architecture, Test for scan circuits, Full serial integrated scan, Multiple scans, Partial scan isolated serial scan, Non-isolated scan.

UNIT VII: Automatic Test Pattern Generation **07**
Digital circuit testing, Testability measures: Controllability, Observability, Basic ATPG, Combinational ATPG Algorithms.

UNIT VIII: Built-In Self-Test **04**
Introduction to BIST concepts, Hardcore, Level of test, Test pattern generation for BIST, Generic off-line BIST architectures, MBIST.

UNIT IX: System-Level Test **03**
Introduction to boundary-scan standards, JTAG 1149.1 standard, TAP/TAM, Introduction to Testing of Memory and IP Cores.

Self-Study:
The self-study content will be declared at the commencement of the semester. Around 10% of the question will be asked from self-study content.

Laboratory Work:

Laboratory work will be based on the above syllabus with minimum of 10 experiments to be incorporated.

Suggested Readings:

1. M. L. Bushnell and V. D. Agrawal-Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Kluwer
2. Janick Bergeron, Writing Test benches-Functional Verification of HDL Models, Springer
3. Miron Abramovici, M. A. Breuer and A. D. Friedman, Digital Systems Testing and Testable Design, John Wiley and Sons/ revised by IEEE
4. Laung-Terng Wang et al., VLSI Test Principles and Architecture, Morgan Kaufman
5. Spear, Chris, Tumbush, Greg, SystemVerilog for Verification A Guide to Learning the Test-bench Language Features, Springer

L = Lecture, T = Tutorial, P = Practical, C = Credit