Institute of Technology, School of Technology, Nirma University, Ahmedabad
Electronics & Communication Engineering Department
M.Tech. Semester-1(VLSI Design, Embedded System)
Schedule of Orientation Program: 28th September to 3rd October 2020

	09:00 a.m. to 9:55 a.m.	10:00 a.m. to 10:55 a.m	2:00 p.m. to 2:55 p.m.	3:00 p.m. to 3:55 p.m.
28/09/2020 (Monday)	Address by Dr. R N Patel (Director, Institute of Technology, Nirma University)[1]	Teaching Scheme and Details of Program (HOD EC)[2]**PMB**	Introduction of VLSI Design (Dr Usha Mehta,PG Coordinator-VLSI Design)[3]**RG**	Introduction of Embedded System (Dr Nagendra Gajjar,PG Coordinator -Embedded System)[4]**RG**
29/09/2020 (Tuesday)	Relaxation Techniques (Dr N P Gajjar, Profesor & PG Coorinator, Embedded Systems, EC Engg. Dept.[5]	Professional Etiquettes (Ms. Cassandra Pillai)[6]	Cross-domain application of Embedded systems(Mr.Rachit Patel, Design Engineer,Intel)*Embedded System Batch [7]**DGS** Job Opportunities in VLSI Domain (Mr.Tapaswi Khamar,Engineer,Intel)*VLSI Design Batch [8]**DJP**	Digital Logic Design(Dr Manish Patel)[9]**DGS**
30/09/2020 (Wednesday)	Academic Regulations (Anand S. Patel)[10]	Scopus - useful tool for Research (Dr S.C.Vora)[11]	Introduction of C,C++ Programming languages (Dr Sachin Gajjar)[12]**VGS**	Introduction to Learning Management System(LMS) and Webex (Dr Vaishali Dhare)[13]**VGS**
01/10/2020 (Thursday)	Writing a Good Research Paper (Dr. P V Bhale,Associate Professor, SVNIT,Surat)[14]	Inter disciplinary Research (Dr S.S.Patel)[15]	Time Management (Dr Dhaval Pujara)[16]	Scope in Embedded Domains (Mitsu Shah, Design Engineer,Intel)*Embedded System Batch[17]**AM** Invention and Evolution of Integrated Circuits (Dr Usha Mehta,PG Coordinator-VLSI Design)*VLSI Design Batch[18]**BDF**
03/10/2020 (Saturday)	University Foundation Day Activity [19]		Digital Signal Processing (Dr Bhupendra Fataniya)[20]**RP**	Health Campus and Drug Awareness (Mr Amit Khare, Intelligence Officer, Narcotics Control Bureau, Ahmedabad)[21]

Google meet link: Slot [1].[5],[6],[10],[11],[14],[15],[16],[19],[21] :: meet.google.com/odn-tsub-qgs
Google meet link: Slot [2].[3].[4],[7],[9],[12],[13],[17],[20] :: meet.google.com/nxr-hsfa-ugm
Google meet link: Slot [8],[18] :: meet.google.com/mza-prbd-qun

Dr Dhaval Pujara
HOD,EC

Dr Nagendra Gajjar
PG Coordinator,Embedded System

Dr Usha Mehta
PG Coordinator, VLSI Design