NIRMA UNIVERSITY
School of Technology, Institute of Technology
B.Tech. Electronics & Communication Engineering
Semester - VII
Department Elective IV

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Course Code	2ECDE10
Course Title	Modern Processor Architecture

Course Outcomes (CO):

At the end of the course, students will be able to –

1. comprehend the design steps for pipelined processors and classify pipelined processors.
2. deploy suitable superscalar technique(s) to enhance the performance of processors for given specifications.
3. recommend suitable data and memory flow techniques to overcome hazards in modern processor architectures.
4. design finite state machine diagram to overcome cache coherence issues in the multiprocessor system.

Syllabus **Teaching hours: 45**

UNIT I: Processor Design **04**

Introduction and evolution, Instruction set processor design, Principles of processor performance, Instruction level parallel processing

UNIT II: Pipelined Processors and Super Scalar Organization **10**

Pipelining fundamentals, Pipelined processor design, Deeply pipelined processors, Limitations of Scalar pipelines, Superscalar pipeline overview

UNIT III: Memory and I/O Systems **04**

Introduction and concept of latency and bandwidth, Memory hierarchy implementation, Virtual Memory systems, Input/output systems

UNIT IV: Super Scalar Techniques **13**

Instruction Flow techniques, Register Data Flow Techniques, Memory data flow Techniques

UNIT V: Multiprocessors and Thread-Level Parallelism **08**

Introduction to Multiprocessor Systems, Symmetric Shared-Memory Architectures, Performance of Symmetric Shared-Memory Multiprocessors, Distributed Shared Memory and Directory-Based Coherence, Explicitly, multithreaded processors

UNIT VI: Case Studies **06**

Recent Modern Processor Architectures, RISC-V Architectures

Self-Study:

The self-study content will be declared at the commencement of the semester. Around 10% of the question will be asked from self-study content.

Suggested Readings:

1. J. Shen and M. Lipasti, Modern processor Design Fundamentals of Superscalar Processors, TMH
2. D. Patterson and J. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Morgan Kaufman
3. William Stallings, Computer Organization & Architecture Designing For Performance, Pearson
4. Behrooz Parahami, Computer Architecture from Microprocessor to Super Computer, Oxford

L= Lecture, T= Tutorial, P= Practical, C= Credit