CERTIFICATE COURSE

ON

TESTING AND VERIFICATION OF VLSI DESIGN

(ONLINE MODE)

DURATION
27-30 OCTOBER 2021 (PHASE-I)
9-12 NOVEMEBR 2021 (PHASE-II)

CONDUCTED BY
DEPARTMENT OF ELLECTRONICS AND COMMUNICATION ENGINEERING,
INSTITUTE OF TECHNOLOGY,
NIRMA UNIVERSITY, AHMEDABAD

NIRMA UNIVERSITY
INSTITUTE OF TECHNOLOGY
NAAC ACCREDITED 'A' GRADE

ABOUT THE PROGRAMME:

The current semiconductor industry has a large demand of manpower in testing and verification field. Considering the job opportunities in this field, mostly all Universities have introduced the courses related to this field in the curriculum of Under Graduate level programs of Electronics and Communication as well as Computer Science. As per a general observation, even though the courses are introduced and students are opting the course, there is a feeling of dissatisfaction at student level because of lack of enough expertise and softwares at many of the Institutes

At Nirma University, we have enough expertize in terms of training faculty members who are known at National level for this field and also enough number of software hardware facilities.

In this scenario, this course targets all those novice industry practitioner and students who want to get mastery of the field Testing and Verification of VLSI Design.

FOR WHOME:

This certificate course is intended for:

- The pre-final and final year undergraduate students and 1st semester onwards of post graduate students from EC, CE, IT, CSE, MSc-IT or equivalent branches can join the course.
- The faculty members who are planning to teach this course with effectiveness
- The research scholars planning to pursue their research in this most exciting field
- Practicing novice engineers who want to migrate to this rewarding field

PREREUISITES:

- Fundamentals of Digital Logic Design
- Basic concepts of Verilog

COURSE MODALITY AND METHOD OF TRAINING:

- Four Days
- Every day: 6 Hrs theory + 2 Hrs Lab session
- It would be a comprehensive e-learning program that provides participants with web-based content, online lectures, online assessment, student performance tracking, hands-on labs, instructor training and support and preparation for industry-standard certifications.

COURSE OUTCOME:

After successful completion of the course, the student will be able to –

1. Select the appropriate tools and methods according to the abstraction level, develop the test bench using functional verification method and apply the static timing analysis.
2. List the possible physical defects, model them as logical faults and determine the test vectors concern to each possible logical fault.
3. Develop scan chain insertion and generate the test set using ATPG tool
4. Develop the Design-for-Test and Built-In-Self-Test circuits as the given application

COURSE CONTENT:

- Introduction: Importance of Testing, Testing during VLSI Lifecycle, Challenges in VLSI Testing, Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology.
- Verification: Importance of verification, Verification plan, Verification flow, Levels of verification, Verification methods and languages
- Functional Verification: Introduction to test bench, Test bench architecture, Types of test benches, case study
- Static Timing Analysis: Concept of Dynamic and Static Timing Analysis, STA for Combinational Circuit and Critical Path, STA for Synchronous Circuit, Set-up and Hold time Violation and its remedies
- Logic and Fault Simulation: Introduction, Simulation Models, Logic Simulation, Fault Simulation
- Automatic Test Pattern Generation: Random and Deterministic Test Pattern Generation, D-Algorithm, Introduction to Advanced ATPG Algorithms
- Design and Testability: Introduction, Testability Analysis, Design for Testability Basics, Scan Cell Designs, Scan Architectures, Scan Design Rules, Scan Design Flow, Special purpose Scan Designs, RTL Design for Testability

RESOURCE PERSONS:

Prof Usha Mehta
PhD in (VLSI Testing)
(Internal Resource Person and Core faculty)
Professor and PG-Coordinator (VLSI Design)
Institute of Technology, Nirma University.
Area of Expertise:
Testing of VLSI Design, Timing Analysis,
SoC-NoC Testing, Hardware Security

Prof Vaishali Dhare
PhD in (VLSI Testing)
(Internal Resource Person and Core faculty)
Assistant Professor (VLSI Design)
Institute of Technology, Nirma University.
Area of Expertise:
QCA Testing, Verification of VLSI Design,
Verilog-System Verilog based Design

TENTATIVE LIST OF EXTERNAL SPEAKERS:

1. Prof. Virendra Singh, IIT Bombay
2. Prof. Santosh Biswash, IIT Guwahati
3. Mr. Tapaswi Khamar, Synopsys, India
4. Ms. Mansi Masrani, Intel, India
5. Mr. Saifee Muffadal, Silicon Engineer, Google, India
6. Mr Viren Gajjar, Synapse Design and Automation, USA
7. Dr Harikrishna Parmar, System Engineer, TCS, India
8. Mr. Jagrat Mehta, Verification Engineer, Eximius Design, India
9. Ms. Radha Tapiawala, Sr. DFT Engineer, Qualcomm, India
10. Dr. Jayesh Popat, freelancer
11. Experts from eInfochips, India
12. Experts from Cadence, India

REGISTRATION FEES: Rs. 3000/- *including 18% Service Tax

Registration fees are non-refundable.

HOW TO APPLY:

The applicants are required to fill the registration form at the following link on or before 24/10/2021. Keep the online transaction details handy while filling the form. Fill the registration form along with transaction details and send a scanned copy to the email ID: kajal.shah@nirmauni.ac.in
https://forms.gle/AnX41bz6i3sAN4wHA

Details for payment of registration fees
Name of the Bank: The Kalupur Com. Co. Op. Bank Ltd
Name of the Beneficiary: Institute of Technology - Under Nirma University
Bank Account Number: 09720180111
IFS Code: KCCB0NRM097

For further details, contact:
Prof. Vaishali Dhare
Email: vaishali.dhare@nirmauni.ac.in
Contact No: +91 9824204333