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Design and analysis of low-power high-speed shared charge reset technique based dynamic latch comparator

Vijay Savani *, N.M. Devashrayee

Electronics and Communication Engineering Department, Institute of Technology, Nirma University, Ahmedabad, India

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ABSTRACT

Circuit intricacy, high-speed, low-power, small area requirement, and high resolution are crucial factors for high-speed and low-power applications like analog-to-digital converters (ADCs). The delay analysis of classical dynamic latch comparators is presented to add more insight of their design parameters, which effects the performance parameter. In this research, a new architecture of dynamic latch comparator is presented, which is able to provide high-speed, consumes low-power and requires smaller die area. The proposed comparator benefits from a new shared charge logic based reset technique to achieve high-speed with low-power consumption. It is shown by simulation and analysis that the delay time is significantly reduced compared to a conventional dynamic latched comparator. The proposed circuit is designed and simulated in 90 nm CMOS technology. The results show that, for the proposed comparator, the delay is 51.7 ps and consumes only 33.62 μW power, at 1 V supply voltage and 1 GHz clock frequency. In addition, the proposed dynamic latch comparator has a layout size of 7.2μm × 8.1μm.

1. Introduction

Data converters, i.e. Analog-to-digital converters (ADC) have become a constituent component which drives the semiconductor industry over the past few years. More and more functional blocks are integrated within a single chip, making this component more conventional and they are able to provide high-speed with low-power dissipation. In addition to these, as most of the devices are becoming portable and battery operated, the features of ADCs like high-speed, low-power, and smaller area on die, make them widely acceptable to the semiconductor industry. All these concerns apply to the most usable representative of the ADCs: the comparator. However, transistor dimension scaling is not straightforward, as it requires gate-induced drain leakage, high channel doping, and band to band tunneling across the junction. Moreover, analog circuit design happens to be more complex to carry out the necessity of reliability, where supply voltages need to be decreased according to the small dimensions of the transistors [1,2]. In ultra-deep sub-micron CMOS technology, the threshold voltage of devices are also not scaled down at the same rate as the technology, which in turn makes comparator design more difficult and challenging at low supply voltage [1–3]. To compensate the reduction in the supply voltage, larger size transistors are used in the design, which in turn increases the power consumption and die size. Another problem in low supply voltage design is switching and input common-mode voltage range. In the literature, various techniques are reported to handle the low voltage design challenges, such as supply boosting technique [4,5], design using body-driven transistors [6,7], current-mode design [8], and using dual-oxide processes. Problem with body driven technique [6] is that, the transistor suffers from low transconductance as its counterpart (i.e. gate driven), it also adds more complexity in the design and fabrication process. For handling low voltage, not only technological advancement, but new circuit architectures can also be developed without adding more complexity in the circuit, to handle such issues in deep sub-micron technology.

Several architectures of high-speed comparators exist, such as the multistage open-loop comparator, the preamplifier latch comparator, and the regenerative latch comparator [1–3]. Among the different structures, high resolution and high speed can be obtained easily by using the multistage open-loop comparator. On the other hand, the latch-type comparator is the most usable clocked regenerative comparators due to its high-speed and low-power consumption. It is based on cross-coupled inverters latch. Latch-type comparators are able to accomplish decisions more rapidly with strong positive feedback and no static power indulgence. In Ref. [9], the author has presented the basic dynamic comparator and two new dynamic comparators, which are based on architectural modification for low-power and high-speed operation. Conventional single tail current dynamic latch comparator is presented in Ref. [10]. In

* Corresponding author.
E-mail address: vijay.savani@nirmauni.ac.in (V. Savani).

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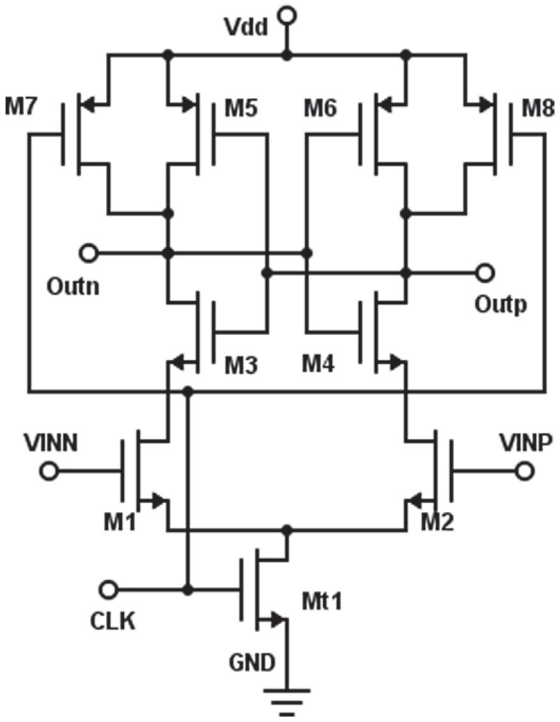

Fig. 1. Single tail current dynamic latch comparator.

Refs. [11,12], the author has presented unique reset technique for the dynamic latch comparator to reduce the delay and power named as shared charge logic. The first double-tail current dynamic comparator proposed in Refs. [13,14] is based on the architectural modification. In this, the author has modified the conventional single tail current dynamic latch comparator in to double tail current latch comparator, where the input and latch stages are separated to operate comparator with lower supply. The architecture level modification to improve speed of the comparator in low supply voltage is also reported in Ref. [15]. In this paper, author has modified the structure of latch into double cross-coupled latch to improve the speed of the dynamic comparator. The broad analysis about the delay of dynamic comparator is presented in Refs. [14–17]. By adding few minimum sized transistors to the conventional double tail current comparator, new dynamic comparators are proposed in Refs. [14–16]. Adaptive power control (APC) technique is reported in Ref. [18], for reduction in the power consumption.

This paper presents detailed analysis of different comparator architecture in terms of delay of dynamic comparator. This paper also discuss the reset schemes of conventional dynamic latch comparator. Based on the concept of shared charge in the reset phase, a new dynamic latch comparator is proposed, which does not require stacking of too many transistors or boosted voltage and can work at low supply voltage. The latch time and ultimately overall delay time is reduced by applying the shared charge logic based reset technique to the double tail current dynamic comparator. As a result of this modification, there is improvement in power and power delay product (PDP) as compared to referred comparators (viz. conventional single tail current, double tail current, modified double tail current and double tail current without inverted clock dynamic latch comparators).

The rest of this paper is organized as follows. The brief functionality and analytical expression of the single tail current dynamic latch comparator and double tail current dynamic latch comparator are presented in section 2. Each of this structure is discussed along with its advantages and disadvantages. Section 3 discusses the reset technique for dynamic latch comparator. Proposed comparator which is based on the shared charge logic based reset technique is discussed and analyzed in this section. Simulation results are presented in section 4, followed by concluding remarks in section 5.

2. Dynamic latched comparators

The strong positive feedback based dynamic latch comparators are preferable as compared to other architectures as they fulfils the requirements of high-speed and low-power ADC. Various performance parameters are analyzed and presented in literature, like noise [19], input referred offset voltage [20–22], kick-back noise [23], and random decision errors [24]. This section presents a comprehensive analysis of delay time for two commonly used topologies (i.e. single tail current dynamic latch comparator (STDLC) and double tail current dynamic latched comparator (DTDLC)) along with their merits and demerits.

2.1. Single tail current dynamic latched comparator (STDLC)

The schematic diagram of a single tail current latched comparator [2,9,10,13,16,25] is illustrated in Fig. 1. The operation of the comparator is divided in two phases: Reset phase (when CLK is low) and regeneration phase (when CLK is high). In the reset phase, M7 and M8 are ON, pulling the output terminals (Outn and Outp) to V_{dd}. Moreover, the tail current source, Mt1 is OFF, which eliminates the static currents from V_{dd} to ground (except the leakage currents which is negligible). In the regeneration phase, the current supply turns ON and the output voltages start to discharge to the ground with different discharging rate, proportional to their corresponding input voltages. The discharge will continue until the gate-source voltage of transistor M5 or M6 reaches under the threshold voltage of M5 or M6 and one of them turns ON. Subsequently, the latch (formed by transistors M3–M6) starts regeneration and forces one output to reach V_{dd} and the other one to the ground.

The transient behavior of the STDLC is depicted in Fig. 2. As shown in Fig. 2, the delay time is divided into two parts t_0 (time for discharging of load capacitance C_L, up to either of M5 or M6 turned ON) and t_{latch} (latch regeneration time). Assuming $V_{INP} > V_{INN}$, the M2 causes faster discharge of output terminal Outp and the t_0 can be found as follows:

$$t_0 = \frac{C_L \cdot |V_{thp}|}{I_2} \cong 2 \cdot \frac{C_L \cdot |V_{thp}|}{I_{t1}}, \quad \left(I_2 \cong \frac{I_{t1}}{2}, for\ small\ value\ of\ \Delta V_{diff} \right) \tag{1}$$

The latch regeneration time is calculated as per equation (2) [1,13]. It is assumed that the comparator is followed by the SR latch which enhances the output to full rail voltage [10] and hence half of the supply voltage is considered to be the threshold voltage ($\Delta V_{out} = V_{dd}/2$).

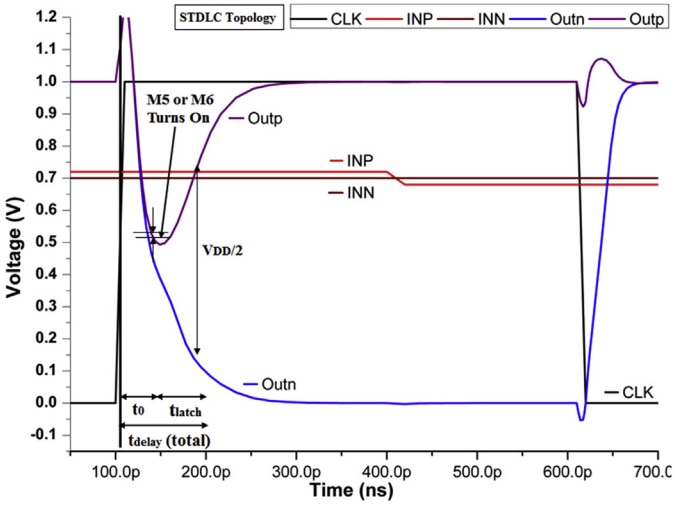

Fig. 2. Transient behavior of the single tail current based dynamic latched comparator topology with $V_{diff} = 20$ mV, $V_{cm} = 0.7$ V, $V_{dd} = 1$ V, and CLK = 1 GHz.

$$t_{latch} = \frac{C_L}{g_{m(eff)}}\cdot\ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) \cong \frac{C_L}{g_{m(eff)}}\cdot\ln\left(\frac{V_{dd}/2}{\Delta V_0}\right) \quad (2)$$

Where $g_{m,eff}$ is the effective transconductance of latch and ΔV_0 is the initial voltage difference which can be calculated as follows by using equation (1).

$$\Delta V_0 \cong 2\cdot|V_{thp}|\cdot\left(\frac{\Delta I_{in}}{I_{t1}}\right) = 2\cdot|V_{thp}|\cdot\sqrt{\frac{\beta_{1,2}}{I_{t1}}}\cdot\Delta V_{diff},\ \left(\Delta I_{in} << I_1\ or\ I_2 \cong \frac{I_{t1}}{2}\right) \quad (3)$$

Replacing ΔV_0 in (2), along with the value of t_0 from (1), the total delay can be written as in equation (4).

$$t_{total} = 2\cdot\frac{C_L\cdot|V_{thp}|}{I_{t1}} + \frac{C_L}{g_{m(eff)}}\cdot\ln\left(\frac{V_{dd}}{4\cdot|V_{thp}|\cdot\Delta V_{diff}}\cdot\sqrt{\frac{I_{t1}}{\beta_{1,2}}}\right) \quad (4)$$

With careful observation of equation (4), the effect of various design parameters can be summarized as follows: (i) the delay is directly related to load capacitance (C_L) and related inversely to differential input voltage (ΔV_{diff}) (ii) the delay indirectly depends on the input common-mode voltage (V_{cm}). There is a tradeoff between smaller and larger tail current. Simulation results show that reducing V_{cm}, finally leads to increase in total delay. In Ref. [10], it has been shown that 70% of the supply voltage is the optimum for the input common-mode voltage as far as yield and speed are concerned (iii) the larger input transistor can be used to minimize the effect of offset, as the load capacitance of these transistor not effecting directly to the speed.

In spite of the zero static power consumption, high input impedance, full swing output, and robustness against mismatch [13,15], this topology has certain draw back as follows: (i) the stack of transistors requires a higher headroom voltage to guarantee all the transistors are working properly. This may be problematic in very low voltage and sub-threshold applications (ii) due to the large voltage swing at the drains of the differential input transistors, it has relatively large kickback noise (iii) the latch current is in common with the input transistors. Thus, increasing the speed is achieved by larger tail current, on the other hand smaller tail current is desirable for the differential stage to keep transistors in week inversion. Therefore, there is a speed-power tradeoff.

2.2. Double tail current dynamic latched comparator (DTDLC)

Fig. 3 shows the schematic diagram of double tail current dynamic latched comparator [13,15,26–29]. As compared to the previous topology, this double tail current latched comparator consists of two stages with two separate current tails. The first stage has a small tail current to achieve low offset whereas the second stage (latch) with a large tail current to provide shorter delay. Similar to the other latched comparator, the double-tail latched comparator works in two phases. During the reset phase (i.e. when CLK is low), the current sources of both stages, Mt1 and Mt2, are switched OFF, ensuring that there is no static power consumption in the first phase. However, M3 and M4 are ON and pulling terminal fp and fn to V_{dd}. As a result, MI1 and MI2 are switched ON and the outputs (i.e. Outn and Outp) are reset to the ground. During the regeneration phase (i.e. when CLK is high), the current sources turn ON, while M3 and M4 are switched OFF. Thus, terminls fp and fn, will discharge with different rate, which is proportional to their corresponding inputs. When one of the outputs of the first stage reaches under the threshold voltage of MI1 or MI2, the intermediate transistor (MI1 or MI2) turns OFF. The positive feedback of the latch starts, forcing one output to reach

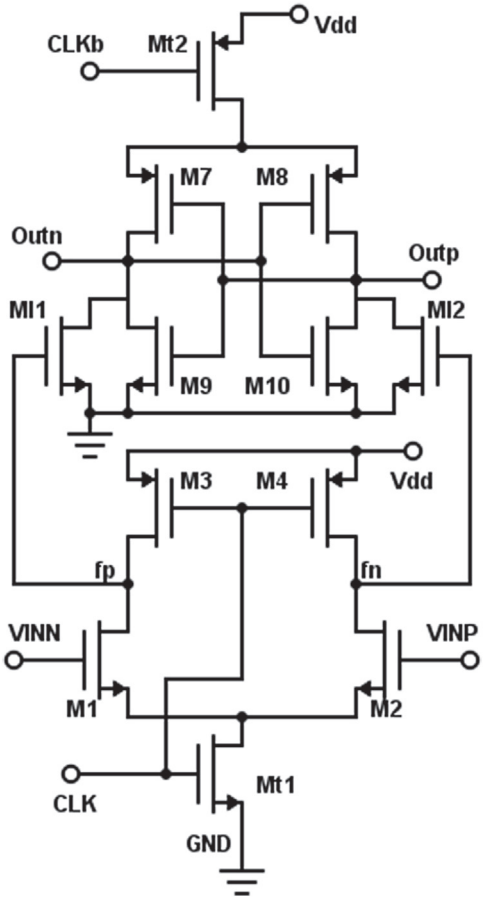

Fig. 3. Double tail current dynamic latched comparator.

V_{dd} and the other one to the ground. The transient behavior is illustrated in Fig. 4.

This comparator also has two parts in delay i.e. t_0 (capacitive discharge of load capacitance till the first nMOS (either M9 or M10) turns ON) and t_{delay} (latch delay). Time t_0 is obtained as follows:

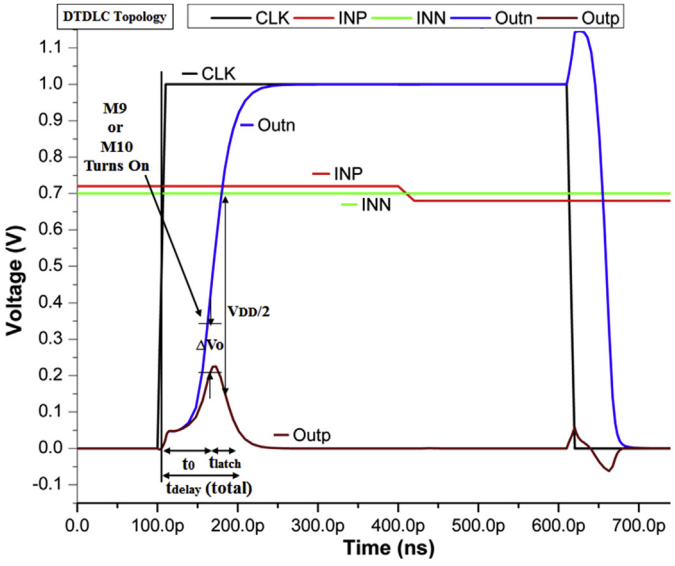

Fig. 4. Transient behavior of the conventional double tail current based dynamic latched comparator with $V_{diff} = 20$ mV, $V_{cm} = 0.7$ V, $V_{dd} = 1$ V, and CLK = 1 GHz.

$$t_0 = \frac{V_{thn}\cdot C_L}{I_{B1}} \cong 2\cdot\frac{V_{thn}\cdot C_{Lout}}{I_{t2}},\ \left(I_{B1} = drain\ current\ (of\ \mathrm{M9}\ or\ \mathrm{M10}) \cong \frac{I_{t2}}{2}\right) \quad (5)$$

Let us assume $V_{INP} > V_{INN}$, after the first nMOS transistor (M9) turns ON, the corresponding output (e.g. Outn) starts discharging to ground, making other side transistor (e.g. M8) to turn ON, charging another output (e.g. Outp) to the supply (V_{dd}). The initial output voltage difference (ΔV_0) at time t_0 is calculated by equation (6). (In this equation I_{B2} and I_{B1} are the right- and left- side branch current of second stage)

$$\Delta V_0 = V_{thn}\cdot\left(1-\frac{I_{B2}}{I_{B1}}\right) \cong 2\cdot V_{thn}\cdot\frac{\Delta I_{latch}}{I_{t2}} = 2\cdot V_{thn}\cdot\frac{g_{mR1,2}}{I_{t2}}\cdot\Delta V_{fn/fp} \quad (6)$$

Where, $\Delta V_{fn/fp}$ is the differential voltage of first stage (between fn and fp at time t_0) and $g_{mR1,2}$ is the transconductance of the transferring stage, made up of transistors MI1 and MI2. This is found as, $\Delta V_{fn/fp} = [t_0\cdot(g_{m1,2}\cdot\Delta V_{diff})]/C_{L,fn(fp)}$. Now, the total delay can be found using equations (2), (5) and (6),

$$t_{delay} = 2\cdot\frac{V_{thn}\cdot C_L}{I_{t2}} + \frac{C_L}{g_{m,eff}}\cdot\ln\left(\frac{V_{dd}\cdot I_{t2}^2\cdot C_{L,fn(fp)}}{8\cdot V_{thn}^2\cdot C_L\cdot g_{mR1,2}\cdot g_{m1,2}\cdot\Delta V_{diff}}\right) \quad (7)$$

General observations from analytical equation (7) are as follows: (i) initial voltage difference (at time t_0) strongly depends on the differential input voltage, latch tail current, capacitive ratio of output to intermediate nodes, transconductance (g_m) of input and intermediate stage transistors and differential voltage between fn and fp at time t_0. If ΔV_0, is increased the delay reduces (ii) once the decision is completed, both the intermediate stage transistors (MI1 and MI2) are cut-off and do not contribute in improving the effective transconductance ($g_{(m,eff)}$) of latch. During reset phase, these nodes need to be charged again to V_{dd}, leading to more power consumption.

3. Proposed shared charge reset technique based dynamic latched comparator (PSCDLC)

3.1. Shared Charge reset technique

In all dynamic latch comparators, two types of reset techniques are used in reset phase to provide valid logical level during evaluation phase. In this reset technique, either output terminals are charged to supply voltage (V_{dd}) or discharged to ground (Gnd) [2,13–16,26–29].

The general idea in the proposed comparator is to use the new reset technique [12] to retain the charge, which helps in reduction of the delay and power. This new technique is called shared charge logic. In this technique, one pass transistor is used in between two output terminals as shown in Fig. 5. Pass transistor (transistor SC) shares the charge between two terminals during reset phase. Because of the charge shared by both the load capacitances, output will not go below the threshold voltage and hence, the input signal can be compared faster during regeneration phase, which speeds up the operation [12]. Due to this technique, significant improvement in delay as well as power reduction is observed and supported by the implementation results.

This shared charge reset technique gives the following advantages in proposed comparator: (i) Output terminal will not go below the threshold voltage and latch would be ON at the start of evaluation phase. Hence, input signal can be compared faster during regeneration phase, which speeds up the operation and reduces the delay (ii) As the output terminals are not require to discharge (to ground) or charge (to supply voltage), there is less power consumption in the design (iii) Use of nMOS instead of using pMOS transistor in latch stage as a tail current transistor, avoids

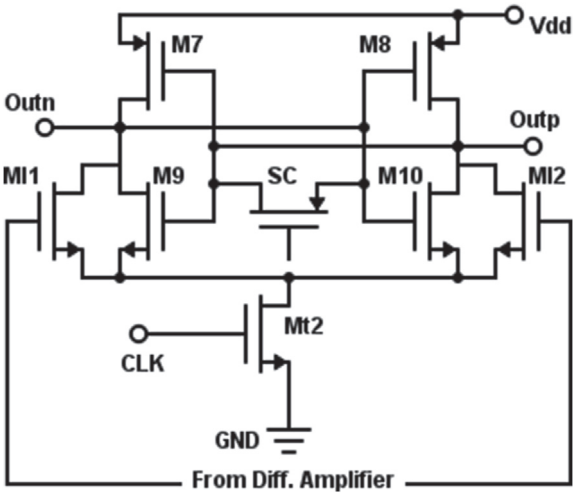

Fig. 5. Shared charge logic in cross-couple latch using pass transistor.

requirement of separate CLK and CLKb (inverted clock) signal. Eventually, it avoids requirement of proper synchronization in-between these two signal to optimize power and delay.

As the double-tail dynamic latch comparator has better performance than that of single tail comparator, proposed comparator is based on the double-tail current comparator. The schematic diagram of the proposed comparator with shared charge logic is shown in Fig. 6 (a).

3.2. Operation of the proposed comparator

The operation of the proposed comparator is divided in two phases, namely reset and evaluation/regeneration phase. During the reset phase (i.e. when CLK is low), the tail transistors of both stages, Mt1 and Mt2, are switched OFF, ensuring that there is no static power consumption in the first phase. During this phase, transistor M3 and M4 are ON and pulling terminals fp and fn are at V_{dd}. As a result, the intermediate transistors MI1 and MI2 are turned ON. In this reset phase, transistor SC shorts output terminals (i.e. Outn and Outp), making it works as a shared charge transistor. This share charge between two terminals (i.e. Outn and Outp), as one of the terminal is at V_{dd} and other is at ground after the previous evaluation phase. In this topology no separate clock control signals are require, as both the tail transistor are of nMOS type.

When the CLK approaches V_{dd}, the circuit enters into evaluation phase. During this phase, the tail transistors Mt1 and Mt2 turn ON, while reset transistors M3 and M4 are switched OFF. Thus, fp and fn, will discharge with different speeds which is proportional to the rate defined by input voltages. Assuming $V_{INN} > V_{INP}$, then fp drops faster than fn. This phenomena would be different, if the opposite condition is assumed for the input voltage. When one of the outputs of the first stage reaches under the threshold voltage of MI1 or MI2, the intermediate transistor (MI1 or MI2) turns OFF. The positive feedback of the latch starts, forcing one output to reach Vdd and the other one to ground. The difference in this architecture functionality is that during evaluation phase decision does not start from two extreme points of voltage level, but both the output terminals are nearly at half of the supply voltage level. Though the initial condition for the output terminal is at half of the supply voltage, it takes lesser time for evaluation and also consumes less power. The delay analysis supports this theoretical concept. The transient behaviour is illustrated in Fig. 6 (b).

3.3. Delay analysis

Theoretical expression for delay has been derived, as it was derived for two previous architectures, in order to demonstrate the effect of shared charge logic in proposed comparator. The method of analysis is similar to the conventional double tail current dynamic latch comparator. Here, in

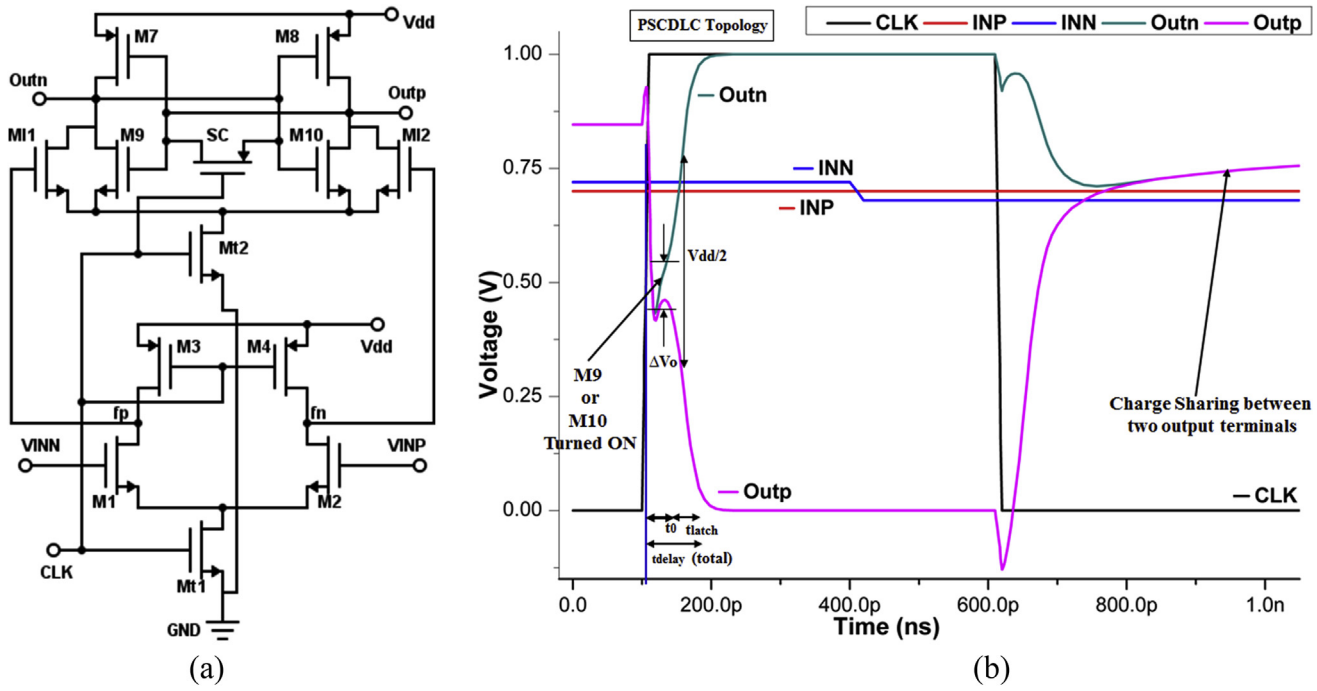

Fig. 6. (a). Schematic diagram of proposed dynamic latch comparator. (b). Transient simulation of proposed dynamic latch comparator with $V_{diff} = 20$ mV, $V_{cm} = 0.7$ V, $V_{dd} = 1$ V, and CLK = 1 GHz.

the proposed comparator architecture, two parameters have been improved, i.e. ΔV_0 at a beginning of regeneration phase and effective transconductance to enhance delay. The total delay is again divided by two terms t_0 and t_{latch}. Term, t_0 is found as per equation (8) as below,

$$\begin{aligned} t_0 &= \frac{C_L \cdot (V_{dd} - 2 \cdot V_{thp})}{I_{B1}} \\ &\cong C_L \cdot \frac{(V_{dd} - 2 \cdot V_{thp})}{I_{t2}} \end{aligned} \tag{8}$$

Where, I_{B1} (or I_{B2} is the drain current of transistor M9 or M10) is approximately equal to $I_{t1}/2$. Similar to double tail current comparator, here ΔV_0 is derived as follows:

$$\Delta V_0 = 2 \cdot (V_{dd} - V_{thp}) \cdot \frac{g_{mR1,2}}{I_{t2}} \cdot \Delta V_{fn/fp} \tag{9}$$

Now, the value of $\Delta V_{fn/fp}$ can be found by equation (10)

$$\Delta V_{fn/fp} = \frac{g_{m1,2} \cdot \Delta V_{diff}}{C_{L,fn(fp)}} \cdot C_L \cdot \frac{(V_{dd} - 2 \cdot V_{thp})}{I_{t2}} \tag{10}$$

Putting the value of $\Delta V_{fn/fp}$ in to equation (9) the value of initial voltage difference ΔV_0 is obtained as follows:

$$\begin{aligned} \Delta V_0 &= 2 \cdot \frac{(V_{dd} - V_{thp}) \cdot (V_{dd} - 2 \cdot V_{thp})}{I_{t2}^2} \\ &\quad \cdot \frac{g_{mR1,2} \cdot g_{m1,2} \cdot C_L}{C_{L,fn(fp)}} \cdot \Delta V_{diff} \end{aligned} \tag{11}$$

Combining equations (8) and (11) to is achieved as t_{total},

$$\begin{aligned} t_{total} &= \frac{(V_{dd} - 2 \cdot V_{thp}) \cdot C_L}{I_{t2}} + \frac{C_L}{g_{m,eff}} \\ &\quad \cdot \ln\left(\frac{V_{dd} \cdot I_{t2}^2 \cdot C_{L,fn(fp)}}{4 (V_{dd} - V_{thp}) (V_{dd} - 2 \cdot V_{thp}) g_{mR1,2} g_{m1,2} C_L \Delta V_{diff}} \right) \end{aligned} \tag{12}$$

Equation (12) is the analytical equation of total delay for proposed comparator.

3.4. Power and PDP

There are various methods are reported in the literature to estimate the power, one of them is time variant modelling of transistors [30,31]. Largely, the average power of supply voltage during one period of comparison is obtained from the well-known formula (13),

$$\begin{aligned} Power_{avg} &= \frac{1}{T} \int_0^T V_{dd} \cdot I_{supply} \cdot dt \\ &= f_{CLK} \cdot V_{dd} \cdot \int_0^T I_{supply} \cdot dt \end{aligned} \tag{13}$$

where f_{CLK} is the clock frequency, V_{dd} is supply voltage, and I_{supply} is the current drawn from the supply. There is atradeoff between speed and power in most circuits. Hence, a better parameter for comparison is the Power Delay Product (PDP). An expression for PDP is derived by multiplying equation (12) and equation (13).

4. Simulation results

The proposed comparator enhances the delay and power parameter as compared to STDLC, DTDLC, and comparators which have been proposed in Fig. 5(a) ref [16] and ref [32,33]. These comparator architectures are referred as, modified double tail current dynamic latched comparator (MDTDLC, Fig. 5(a) [16]) and double tail dynamic latch comparator without inverted clock (DTDLC-CLK, [32,33]). In order to compare the proposed comparator with the STDLC, DTDLC, MDTDLC (Fig. 5(a) [16]) and DTDLC-CLK [30,31]), all circuits have been implemented and simulated in 90 nm CMOS technology with supply voltage (V_{dd}) of 1 V, input common-mode voltage (V_{cm}) of 20 mV and clock frequency (CLK) of 1 GHz using Virtuoso Tool and SPECTRE simulator. Optimization of the transistor dimensions were done to get an equal offset standard variation of 7.7 mV at the input common mode voltage of 0.7 V. The delay, power and power delay product are the basic performance parameters of the comparator. The influence of input differential voltage on

Table 1
. Summary of the comparators performance.

Comparator Architecture	Number of Transistor	Delay (ps)	Power (μW)	PDP (fJ)	Delay/log(V_{diff}) (ps/*decade*)	Energy per Conversion (fJ)
STDLC	9	77.7	26.89	2.09	40.12	26.9
DTDLC	14	66.4	52.40	3.48	27.36	52.4
MDTDLC	16	54.5	147.70	8.05	27.31	147.7
DTDLC-CLK	17	75.40	57.20	4.31	28.9	57.2
PSCDLC	13	50.9	31.80	1.62	26.9	31.63

V_{diff} (ΔV_{in}) = 20 mV, V_{cm} = 0.7 V, V_{dd} = 1 V, and CLK = 1 GHz

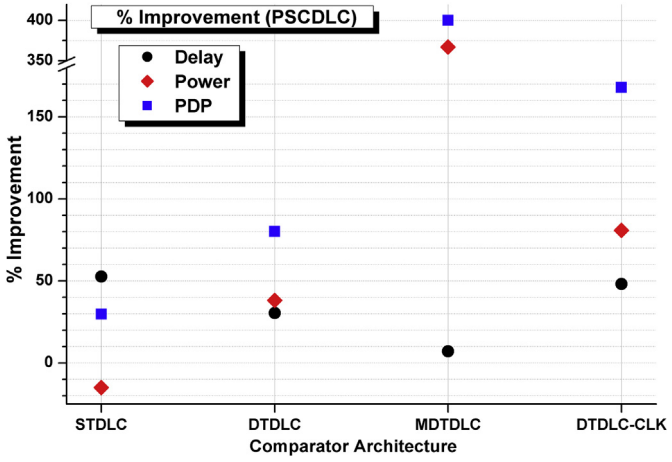

Fig. 7. Percentage (%) improvement in performance parameter for proposed comparator as compared to referred comparator architectures.

delay (Delay/log(V_{diff})) and Energy per conversion (Eng./Conv.) are the two other important parameters for the comparator. For better comparison all these parameters are calculated for previously mentioned architectures (referred comparator) along with proposed comparator and the results are summarized in Table 1. Fig. 7 show percentage improvement in the three basic parameters for proposed comparator as compared with referred comparator architectures. Table 2 shows the summary of various parameter results for proposed comparator.

To get more insight of the comparator performance, simulation of variation parametric/input signals sweeps are carried out. Tables 3 and 4 summarizes the simulation results of performance parameters (i.e. delay and PDP) for the referred comparator along with proposed comparator versus input differential voltage, respectively. It is observed from Table 3, that the delay of the proposed comparator is lowest for all range of input differential voltage as compared to reffered comparators. As far as the power consumption and PDP are concerned, it also remains lowest in all ranges of input differential voltage for proposed comparator, as shown in Table 4. Fig. 8 shows effect of input differential voltage on energy per conversion. It is being observed that the proposed comparator has somewhat more energy per conversion as compared to STDLC, whereas compared to other double tail comparators architectures, it is significantly reduced.

Simulations to observe the effect of supply voltage on the performance parametersare carried out for the proposed comparator and referred comparator. The simulation results for delay, PDP, and Energy/Conv. are shown in Fig. 9 (a)–(c) respectively. With input common mode voltage (V_{cm}) of 0.7 V and input differential voltage (V_{diff}) of 20 mV, the proposed comparator has less delay time in comparison to the conventional one in all ranges of supply voltage as observed from Fig. 9 (a). Fig. 9(c) shows the influence of supply voltage on energy per conversion for all the comparators and it shows that the energy per conversion for the proposed comparator is comparable with the existing architectures.

Commonly, in the double-tail current topologies, the delay of the comparator is less affected by the deviation of the input common-mode voltage as compared to other comparator architectures and thus has a wider common-mode range. Table 5 shows the effect of input common

Table 2
Pre-Layout performance of proposed comparator.

Parameter	Value
Technology	90 nm CMOS
Supply Voltage (V)	1
Power Dissipation (μW)	31.80
Operating Frequency (GHz)	1
Delay (ps)	50.9
Power Delay Product (PDP) (fJ)	1.62
Offset Voltage (mV)	7.7
ICMR (V)	0.1–0.7

Table 3
Effect of input differential voltage on delay for various comparator architectures.

V_{diff} (mV)	Comparator Topologies, *Delay*(ps)				
	STDLC	DTDLC	MDTDLC	DTDLC-CLK	PSCDLC
5	105.6	84.0	71.4	97.7	**67.5**
10	93.4	75.7	81.0	85.4	**59.2**
20	77.7	66.4	71.7	74.8	**50.9**
40	69.0	58.1	63.6	64.9	**42.7**
50	65.0	55.6	61.3	61.8	**40.1**
100	53.2	48.4	53.7	53.4	**32.3**
200	43.5	42.2	46.8	47.1	**25.6**

Vcm = 0.7V, Vdd = 1V, Clk = 1 GHz

Table 4
Effect of input differential voltage on PDP for various comparator architectures.

V_{diff} (mV)	Comparator Topologies, *PDP*(fJ)				
	STDLC	DTDLC	MDTDLC	DTDLC-CLK	PSCDLC
5	3.3	4.6	10.7	5.8	**2.3**
10	2.8	4.8	11.7	5.0	**1.9**
20	2.2	4.1	10.2	4.3	**1.6**
40	1.8	3.5	8.9	3.7	**1.3**
50	1.7	3.4	8.5	3.5	**1.2**
100	1.3	2.8	7.4	3.0	**0.9**
200	1.0	2.3	6.0	2.7	**0.7**

Vcm = 0.7V, Vdd = 1V, Clk = 1 GHz

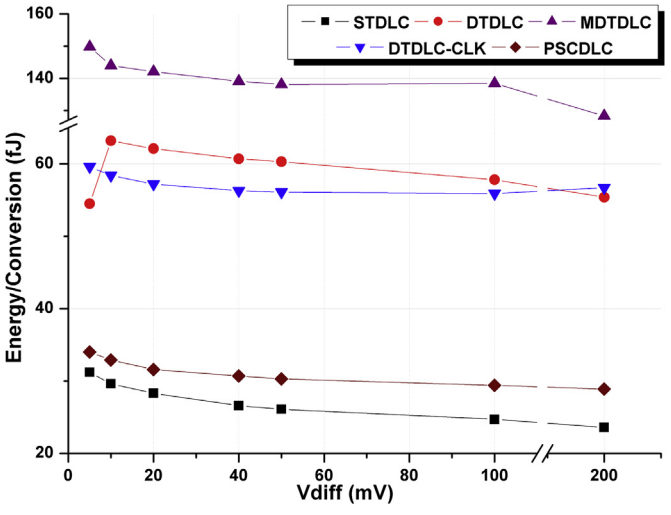

Fig. 8. Effect of input differential voltage on Energy/Conversion for proposed and referred comparator.

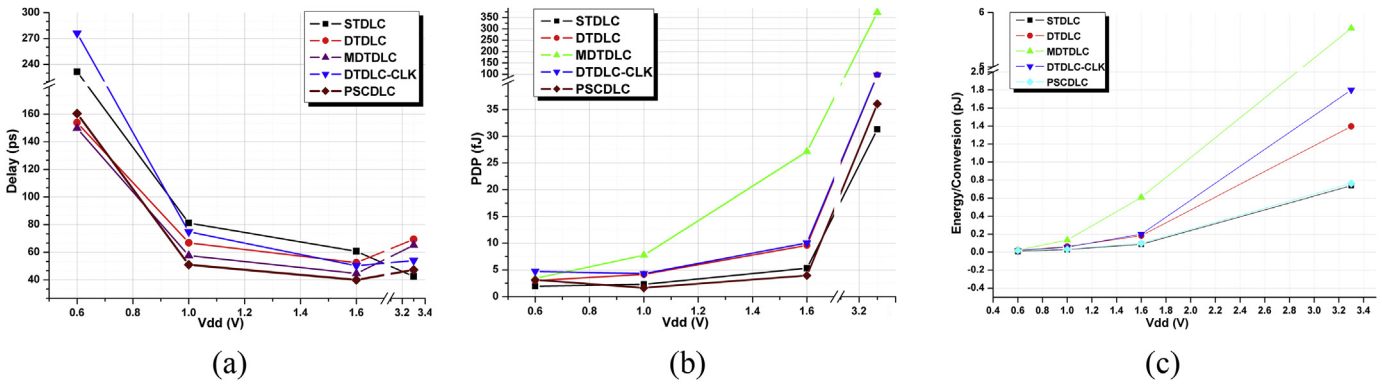

Fig. 9. Effect of supply voltage on (a) Delay, (b) PDP, and (c) Energy/Conversion for proposed comparator as compared to referred comparator architectures.

voltage on delay for referred comparator along with the proposed comparator. The delay is varying in the range 74–364 ps, 72–191 ps, 56–125 ps, and 72–195 ps for STDLC, DTDLC, MDTDLC, and DTDLC-CLK, whereas in the proposed comparator this range is 53–61 ps and it is not varying too much, which shows that delay is almost constant for a wide range of input common-mode voltage. For the range of the input common mode voltage i.e. 0.3 V–0.8 V, the delay remains almost constant which is in the range of 60–53 ps. The PDP is also observed lowest and almost remains constant for a wide range of input common mode voltage. The summary of simulated performance (Energy/conversion) as a function of input common voltage (V_{cm}) is listed in Table 6.

To perceive the effect of input differential voltage on the concerned parameter with different supply voltage, simulation is performed with different input differential voltage with a range of supply voltage with *V*cm of 0.7 V and CLK frequency of 1 GHz. Fig. 10 demonstrates the results of delay for these variations. It is being observed that the delay remains in the range of 26–67 ps with variation in the input differential voltage of 200–5 mV with a supply voltage of 1 V. For the other two levels of supply, it is varying in the range of 366–512 ps and 21–52 ps for the supply voltage of 0.6 V and 1.6 V respectively. Simulations are carried out for proposed comparator for the performance parameters as a function of input differential voltage at different common-mode voltage levels with supply voltage (V_{dd}) of 1 V and clock frequency of 1 GHz. Table 7, shows pre-layout simulated delay versus input differential voltage in the proposed comparator at different common-mode voltage levels and it is graphically demonstrated in Fig. 11. The delay remains moderate and comparable for the input common-mode voltage in the range of 0.4–0.7 V. It is reducing as the differential input voltage reduces. Table 8 shows the dependence of PDP on common-mode voltage at various differential input voltage and the same is depicted in Fig. 12 for proposed comparator. Furthermore, the energy per conversion also remains persistent in this range as observed from Fig. 13. The range of the input common mode voltage for the optimum value of performance parameters in proposed comparator is from 0.5 V to 0.7 V.

The effect of differential input voltage on delay and PDP at various supply voltage for proposed comparator is simulated and the results are demonstrated in Figs. 14 and 15 respectively.

To verify the effectiveness of proposed comparator, pre-layout and post-layout simulation is carried out for STDLC, DTDLC, MDTDLC (Fig. 5(a) [16]) and PSCDLC (proposed architecture). Fig. 16 shows schematic layout of the proposed comparator. Comparison of Post-Layout simulation results for proposed comparator as compared to referred comparator is presented in Table 9. It is being observed that approximated area requirement by proposed comparator is comparable or least as compared to referred architectures. Pre- and Post- Layout yield is calculated as a function of input differential voltage and its results comparison is shown in Fig. 17.

As the technology is shrinking and complexity is increasing in

Table 5
Effect of input common voltage on delay for different comparator architectures.

Vcm (V)	Comparator Architectures, *Delay* (ps)				
	STDLC	DTDLC	MDTDLC	DTDLC-CLK	PSCDLC
0.3	364.5	191.2	125.8	195.3	**60.9**
0.4	158.0	114.4	70.1	118.4	**48.0**
0.5	102.5	87.9	55.8	89.8	**46.9**
0.6	84.4	77.0	53.4	79.0	**48.8**
0.7	77.7	72.8	54.3	74.9	**50.9**
0.8	74.8	72.5	56.6	72.3	**52.9**

$V_{diff} = 20$ mV, $V_{dd} = 1$ V, and CLK = 1 GHz

Table 6
Effect of input common voltage on Energy/Conversion for different comparator architectures.

V_{cm} (V)	Comparator Architectures, Energy/Conv.(pJ)				
	STDLC	DTDLC	MDTDLC	DTDLC-CLK	PSCDLC
0.3	0.0180	0.1044	0.1199	0.2089	**0.0523**
0.4	0.0241	0.0624	0.0966	0.0823	**0.0342**
0.5	0.0247	0.0502	0.1237	0.0543	**0.0315**
0.6	0.0258	0.0455	0.1411	0.0452	**0.0313**
0.7	0.0269	0.0437	0.1474	0.0428	**0.0318**
0.8	0.0282	0.0434	0.1513	0.0412	**0.0326**

$V_{diff} = 20$ mV, $V_{dd} = 1$ V, and CLK = 1 GHz

Table 7
Summary of delay of the proposed comparator as a function of input voltage difference with different input common-mode voltage.

V_{diff} (mV)	Input Common mode Voltage - V_{cm} (V) [*Delay* (ps)]					
	0.3	0.4	0.5	0.6	0.7	0.8
5	84.23	64.87	63.69	65.53	67.54	69.52
10	72.74	56.60	55.20	57.18	59.18	61.14
20	60.85	48.02	46.88	48.81	50.90	52.90
40	48.91	39.26	38.72	40.52	42.67	44.64
50	45.13	36.53	36.11	37.93	40.08	42.03
100	34.31	28.89	28.74	30.28	32.30	34.30
200	25.72	23.26	22.84	23.95	25.62	27.56

$V_{dd} = 1$ V and CLK = 1 GHz

Table 8
Summary of PDP of the proposed comparator as a function of input voltage difference with different input common-mode voltage.

Input differential Voltage [V_{diff}(mV)]	Input Commonmode Voltage - V_{cm} (V) [*PDP* (fJ)]					
	0.3	0.4	0.5	0.6	0.7	0.8
5	4.74	2.36	2.15	2.19	2.32	2.42
10	3.98	1.99	1.79	1.85	1.95	2.06
20	3.18	1.64	1.48	1.53	1.62	1.73
40	2.39	1.29	1.18	1.22	1.31	1.41
50	2.15	1.19	1.09	1.13	1.22	1.31
100	1.49	0.90	0.84	0.88	0.95	1.04
200	1.06	0.70	0.65	0.68	0.74	0.81

$V_{dd} = 1$ V and CLK = 1 GHz

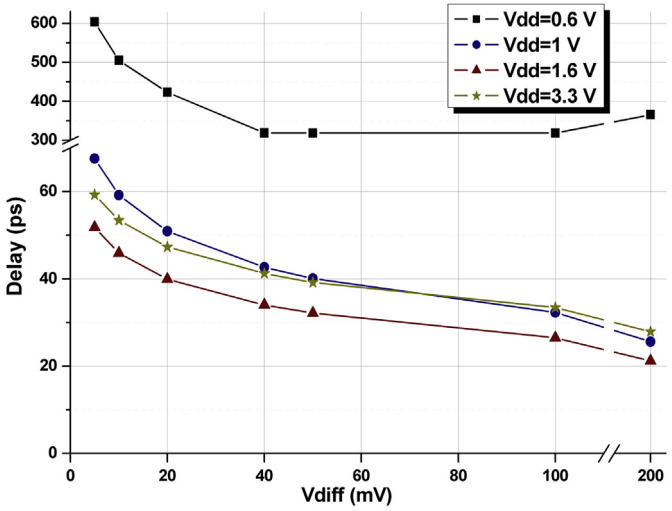

Fig. 10. Simulated results of the delay v/s. supply voltage at various input differential voltage levels with $V_{cm} = 0.7$ V and CLK = 1 GHz.

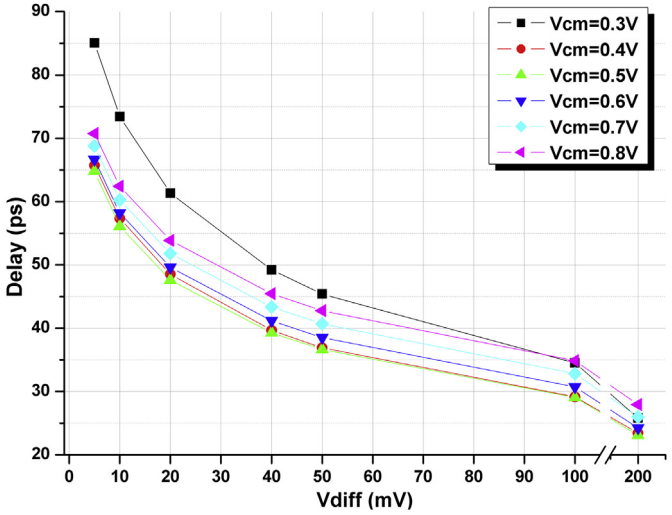

Fig. 11. Simulated results of the delay v/s. input differential voltage at different input common mode voltage with $V_{dd} = 1$ V and CLK = 1 GHz.

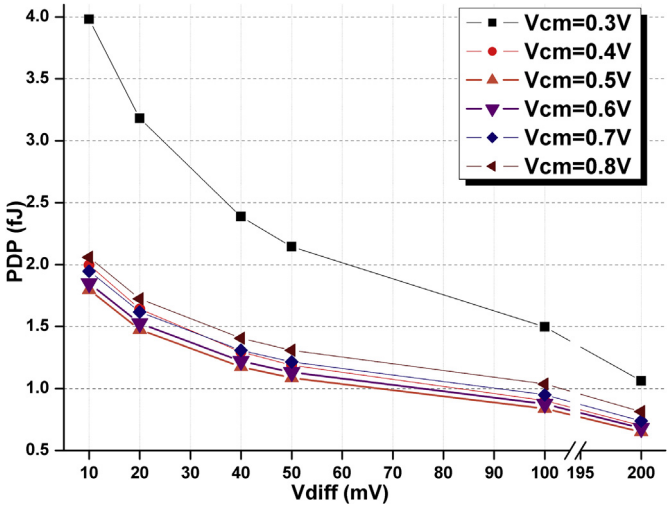

Fig. 12. Simulated results of the PDP v/s. input differential voltage as a function of input common mode voltage with $V_{dd} = 1$ V and CLK = 1 GHz.

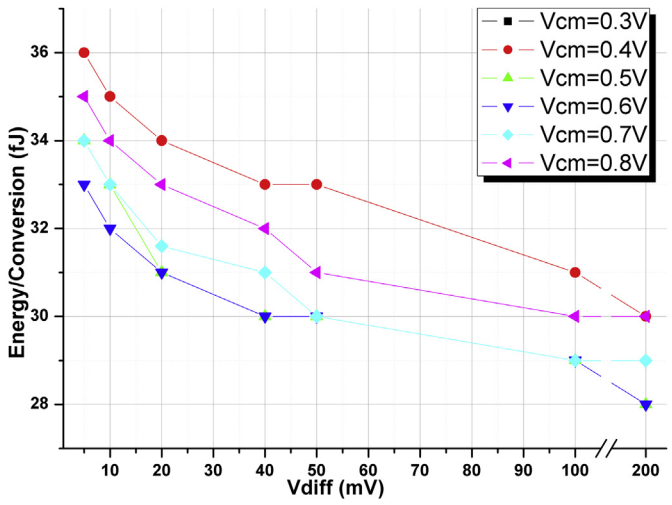

Fig. 13. Simulated results of the Energy/Conversion v/s. input differential voltage as a function of input common mode voltage with $V_{dd} = 1$ V and CLK = 1 GHz.

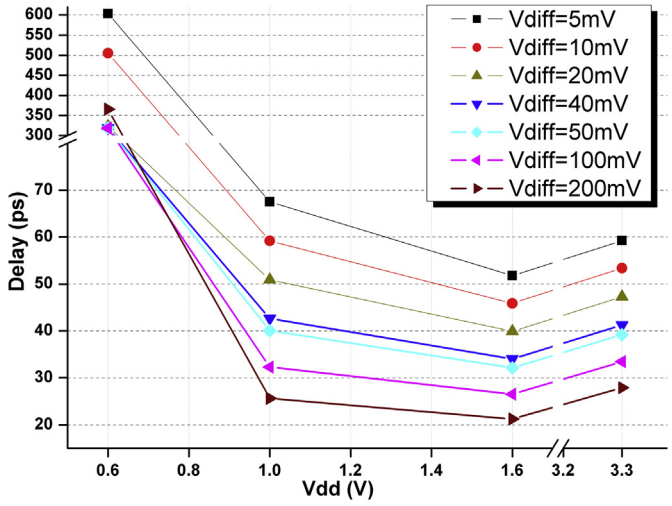

Fig. 14. Simulated results of the delay v/s. supply voltage as a function of input different differential voltage with $V_{cm} = 0.7$ V and CLK = 1 GHz.

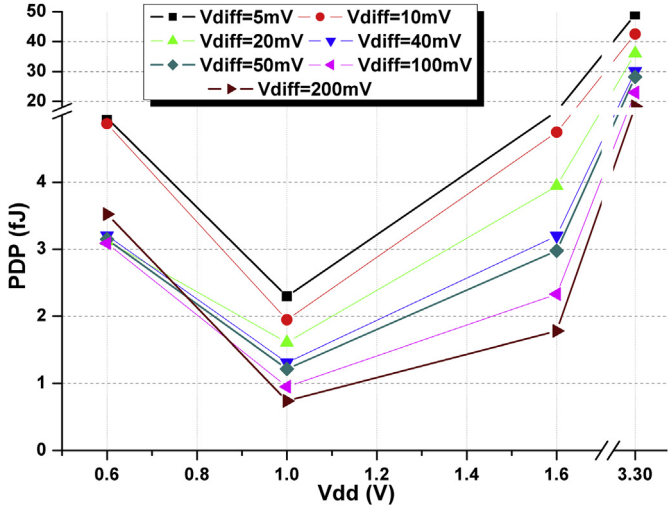

Fig. 15. Simulated results of the PDP v/s. supply voltage as a function of input different differential voltage with $V_{cm} = 0.7$ V and CLK = 1 GHz.

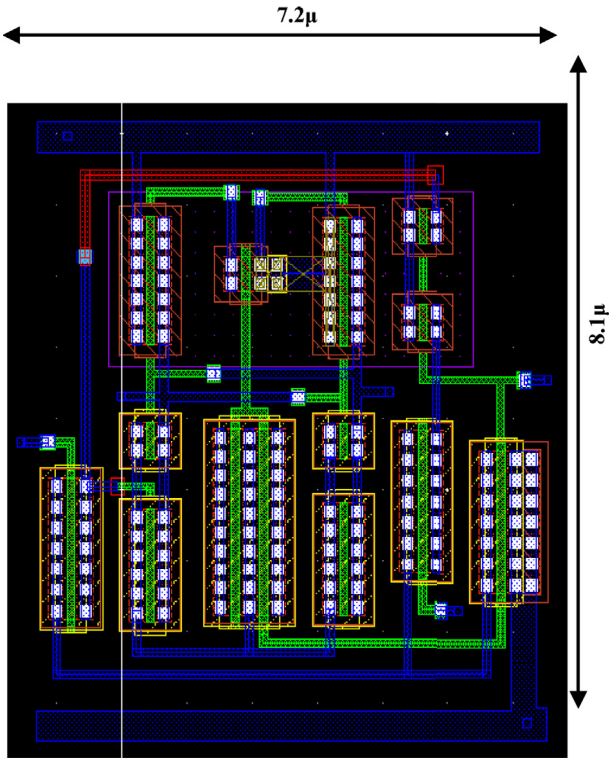

Fig. 16. Layout of proposed comparator.

Table 9
Post- layout performance comparison.

Comparator Architectures	Delay(ps)	Power (µW)	PDP (fJJ)	Layout Area (µm^2)	Energy/ Conversion (fJ)
STDLC	84.4	28.30	2.39	7.23 × 7.575	28.3
PSCDTC	72.8	52.40	3.81	7.84 × 7.15	52.4
MDTDLC	72.7	154.10	11.20	8.99 × 9.295	154.1
PSCDLC	51.8	32.62	1.69	7.2 × 8.1	32.6

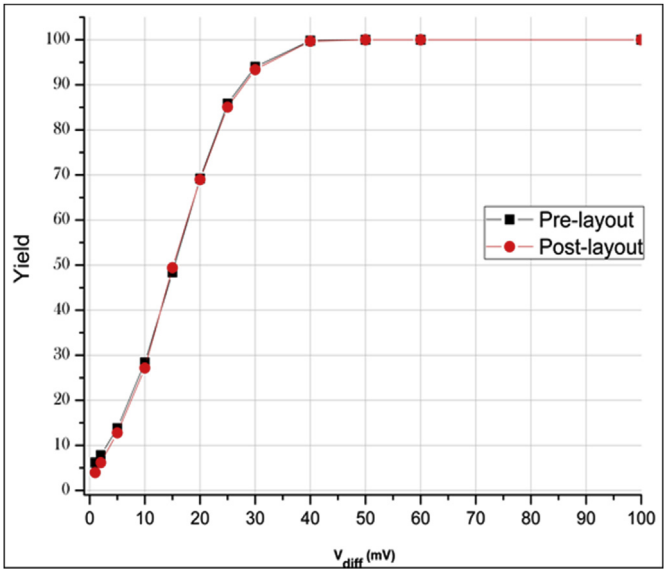

Fig. 17. Yield comparison for proposed comparator (pre-layout and post-layout) as a function of differential voltage.

fabrication, all the comparators have been simulated (pre-layout and post-layout) in various process corners (FF, FS, NN, SF, and SS). Figs. 18 and 19 shows comparison of effect of process corner variation (Pre- and Post- Layout) on (a) Delay (b) PDP for proposed comparator with referred comparator respectively. The result affirms that the performance parameters of the proposed comparator are not varying much across the all four process corners.

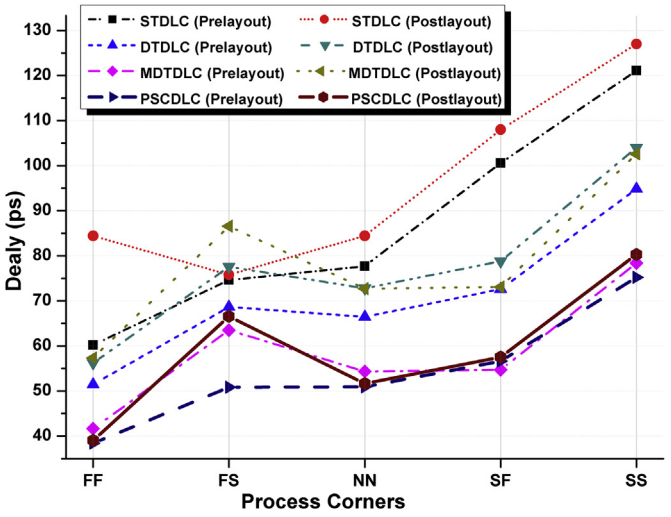

Fig. 18. Comparison of effect of process corner variation (Pre- and Post-Layout) on Delay for proposed comparator with referred comparator.

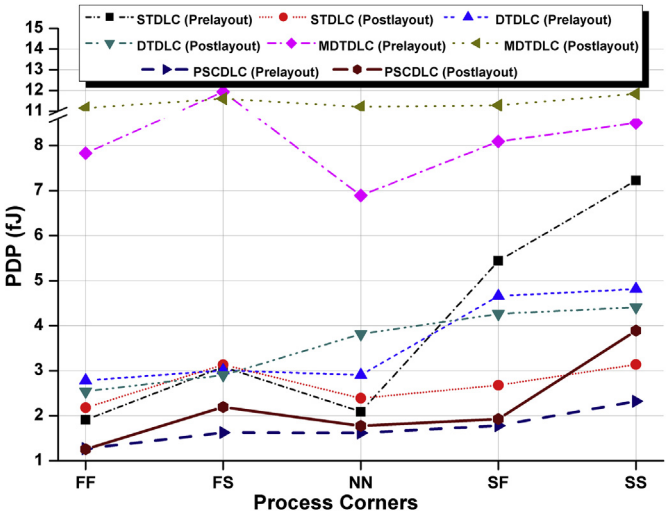

Fig. 19. Comparison of effect of process corner variation (Pre- and Post-Layout) on PDP for proposed comparator with referred comparator.

Table 10
Performance summary of the proposed comparator.

Item	Value
Technology	90 nm CMOS
Supply Voltage (V)	1
Clock Frequency (GHz)	1
Number of Transistors	13
Delay (ps)	51.76*s*
Power (µW)	32.62
PDP (fJ)	1.69
Estimated area (µm^2)	7.2 × 8.1
Energy per conversion (fJ)	32.6
FoM (fJ/Conv)	0.5

Table 11
Performance comparison.

Comparator Properties	[13]	[15]	[26]	[16]			[27]	[28]	[29]	Present Work (PSCDLC)
Year	2007	2009	2013	2014			2015	2016	2016	–
				ST	DT	MDT				
Technology (nm)	90	65	180	180	180	180	65	180	180	90
Supply Voltage (V)	1.2	1.2/0.65	0.5	0.8	0.8	0.8	0.6/0.9	0.6	0.8	1
Clk Frequency (Hz)	1 G/2 G	5 G/0.6 G	5 M	900 M	1.8 G	2.4 G	1.3 G/3.3 G	100 K	1.66 G	1 G
Number of Transistor	12	13	9	9	14	16	26	16	20	13
Delay (s)	20 p	104 p/650 p	16.4 n	940 p	358 p	294 p	–	8.3 n	761 p	51.76 p
Power (W)	113 µ/225 µ	2.88 m/128 µ	20.2 n	0.27 m	0.486 m	0.576 m	64 µ/472 µ	1.56 n	694 µ	32.62 µ
PDP (fJ)	2.3	299/83.2	0.33	253.8	173.9	169.3	49.2/143	0.0129	528.2	1.69
Estimated area (μmxμm /μm^2)	11×7.5	28.4×49.1	–	16×16	28×12	28×14	265	–	–	7.2×8.1 / 58.32
Energy per conversion (fJ)	113	576	–	300	270	240	49/143	15.6	418	32.6
FoM (fJ/Conv)	0.75	2.91	–	5.9	5.3	4.6	1.25/0.94	0.39	7.5	0.5

Monte Carlo simulations are carried out for 500 runs on delay time and power consumption given the process variations along with mismatch variation. The average value of the delay of the proposed comparator is achieved to be 53.19 ps using Monte Carlo simulation. The process variations give a standard deviation of 8.73 ps in delay time. This shows that the delay is not significantly influenced by the process variation. The average value of the power consumption and the standard deviation is 31.89 µW and 466.2 nW. This again shows that the power consumption is also not significantly influenced by the process variation.

The performance evaluation is carried out for the proposed comparator with various state of the art comparator architectures using well identified figure of merit (FoM) [30]. To measure the performance of the design, the FoM is calculated by means of following equation (14):

$$\text{FoM} = \frac{P_d}{2^n \cdot f_s} \tag{14}$$

Where, P_d, is the power dissipation, n is the number of bits (resolution, which has a direct relation with the offset voltage and calculated for 0.5 LSB resolution, and f_s is the maximum sampling frequency) of the comparator. Table 10, summarizes the performance of the proposed dynamic comparator.

Table 11, compares the performance of the proposed comparator with the conventional dynamic comparators. In 90 nm CMOS process parameter, the proposed comparator provides the maximum sampling frequency of 3.9 GHz at 1 *V* supply voltage.

5. Conclusion

In this paper, a detailed analysis of the delay time for the conventional and proposed dynamic latch comparator is presented. The different reset techniques for the dynamic latch comparator is discussed and new shared charge based reset technique is proposed to improve the performance parameter of the comparator. A new low-power, high-speed, and low voltage dynamic latch type comparator based on this reset technique is presented in this paper. Simulation is carried out in 90 nm CMOS technology and the result confirms that performance parameters i.e. delay, power, and PDP are improve to a great extent. The lowest delay is observed by the proposed comparator. It has 53 %, 30 %, 7 % and 48 % improvement in terms of delay as compared to STDLC, DTDLC, MDTDLC and DTDLC-CLK architectures, respectively. Percentage improvement in PDP for the proposed comparator is 30 %, 80 %, 399 % and 167 % as compared to single tail, double tail, comparator of ref [16], and comparator of ref [30,31] respectively. Parametric analysis is also carried out and it confirms that the performance parameter of the proposed comparator is not varying with process variation. To support analytical results, pre-layout and post-layout simulation along with process corner variation is carried out. Monte Carlo simulations are carried out given the process variations along with mismatch variation. The process variations give a standard deviation of 8.73 ps in delay time. The average value of the power consumption and the standard deviation is 31.89 µW and 466.2 nW. The corner analysis and the Monte Carlo simulation results clearly reveal that in proposed the dynamic latch comparator, the delay and power is not varying significantly. It confirms that the proposed comparator is giving best architecture as far as delay, PDP and area is concerned.

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