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Design for Improving Non-Linearity Error of Current Steering DAC for Biomedical Applications

Jayeshkumar J. Patel,
Research Scholar, Institute of Technology, Nirma University, Ahmedabad
Dr. Amisha Naik
Associate Professor, Institute of Technology, Nirma University, Ahmedabad

Abstract

A compact current-mode Digital-to-Analog converter (DAC) suitable for neural stimulator based artificial retinal prostheses is represented in this paper .The designed DAC is binary weighted in 180nm CMOS technology with 1.8V supply voltage. In this implementation the authors have calculated for DAC having various type of switches: NMOS, PMOS switch and Transmission Gate. The implemented DAC uses lower area and power compared to unary architecture due to absence of digital decoders. The desired value of Integrated non linearity (INL) and Differential non linearity (DNL) for DAC for Artificial Retinal Prostheses are of ±0.5LSB. Result obtained in this works for INL and DNL is ±0.34LSB and ±0.38 LSB respectively with 22mW power dissipation.

Keywords: *DAC, DNL, INL, Digital-to-analog converter, CMOS current-steering DAC, Low power, Transmission Gate, SFDR,*

INTRODUCTION

The Digital to Analog converter is a circuit which converts digital signal into analog one. It is widely used in digital signal processors. DACs are often used to convert finite- precision time series to a varying physical data. These are mainly used in different applications like data distribution & acquisition systems amplifier, Electronics display etc…

The Current steering DAC's are the more commonly used architectures because of their small size and simplicity, high resolution and high speed. 6-bit binary weighted are the inputs of architecture. Based on the binary principle current sources are scaled. Here the i^{th} current source output current is equal to the 2^i.I, Where I = ILSB, i.e., least significant bit (LSB) current. For the design of DAC, we used the Transmission Gate and PMOS switches.

Here for 4-bit converter, the 4 weighted current sources are used, those are represented as: I_o, $2I_o$, $4I_o$ and $8I_o$. The main advantage of this architecture is number of current cells required will be reduced hence this architecture is most suitable for higher resolution implementations. The disadvantage with this architecture is it produces higher amount of glitches (unwanted signal) on the contrary the unary architecture offers higher accuracy with greater linearity at the cost of chip area and power overhead.

DAC is a crucial part of the retinal Prostheses. Parameters like non linearity error which includes INL & DNL, power dissipation, conversion time etc. play an important role. Characteristics of switching elements are one of the prominent factors for such parameters.

ARTIFICIAL RETINAL PROSTHESES

The matter of the retinal prostheses is represented in Figure 1. The external camera is used to capture the image. The image information is converted into associated analog signal. The chip is implanted in the retina, converted signal is fed to the chip by wireless media. The chip offers artificial vision by the process of stimulation and same is available to retinal cells. Various Experiments have been carried out with different laboratory settings & Patients. So far, blind patients can read large fonts using prostheses. However, the perceptual resolution of current systems is quite low.

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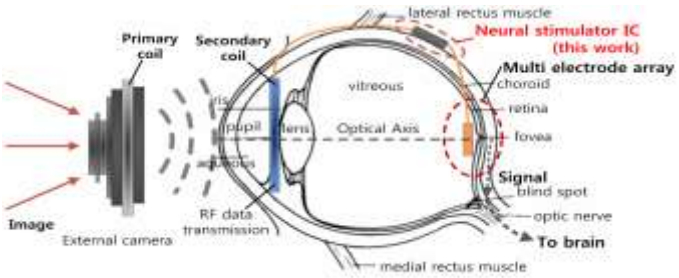

Figure 1. Concept of artificial retinal prostheses.[4]

The system level design of Proposed DAC is represented in Figure 2. It is a part of multichannel DAC with Electrode for each pixel circuits. Using the concept of sharing, the pixel size can be reduced. This will be more prominent as the number of pixel is increased for higher resolution.

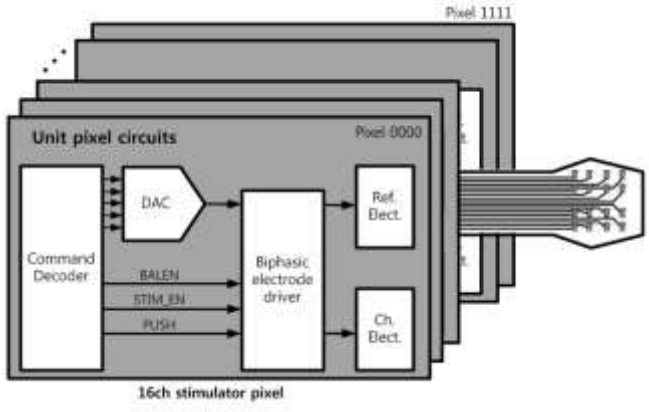

Figure 2 System level architecture of stimulator IC.

CURRENT STEERING DAC

A 4-bit binary weighted current steering DAC is designed and implemented with various switching approaches suitable for retinal prostheses application. Though this architecture occupies lesser digital area and power, but suffers from lower performance. The authors have calculated INL, DNL of 4-bit Binary Current Steering DAC with the help of NMOS, PMOS and Transmission Gate Switch.

N-bit DAC is represented as below shown in Figure 3.

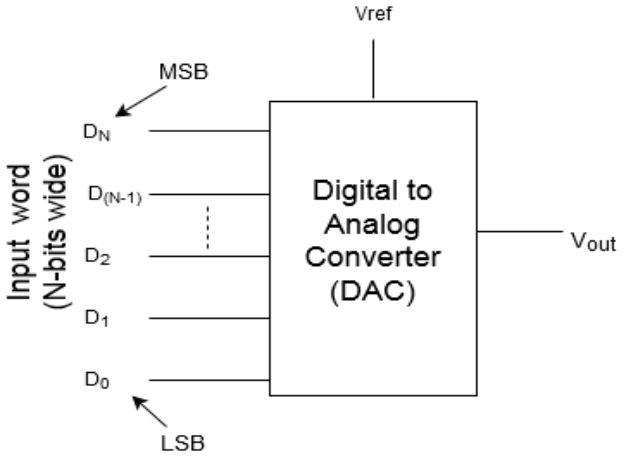

Figure 3 N-bit DAC representation

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For N-bit DAC, output is expressed as follow:

$$V_{OUT} = \left(D_{N-1}\,2^{N-1} + \ldots + D_0\,2^0\right)\frac{V_{REF}}{2^N}$$

$$V_{OUT,\max} = \frac{2^{N-1}}{2^N}\cdot V_{REF}$$

Compared to other Architecture i.e. R-2R ladder DAC, weighed resistor DAC and Capacitive DAC; Current steering DAC is faster and low power consuming. There is no need of extra buffer to drive a load. A current steering DAC uses a reference current source. The source is replicated in each branch of DAC. The current sources belongs to the branch is switched on or off according to digital inputs. In case of binary weighed current steering DAC, Current source having the value of 2^N*Io. Where Io is reference current. No. of switches are same as no. of current sources and same as N. Based on ON/OFF of current sources, total current is added and it will be the output current. Switches are MOS switches- NMOS, PMOS or Transmission Gate and sane are controlled directly by digital inputs. Output current is as per input code.

The characteristics of Switch play an important role for high speed, low power and high resolution DAC. Which decides the Non linearity say DNL and INL of DAC.

There are other architectures in implementation say unary current steering DAC. Said architecture is complex in terms of number of current sources. Here each current sources have the same value of Io (reference current) but number of current sources are ((2^N)-1) and same no. of switches as well. It offers advantage in form of less glitches but required more area. It is also required to have additional hardware to convert binary code into thermometer code.

Looking to implementation, area efficiency and free from additional hardware for binary to thermometer code conversion, Binary current steering DAC structure is the simplest one. N bit configuration which needs only N current sources. They are straightforwardly worked by the linear binary input codes. However, due to the inadequate synchronization of the switches and dynamic behavior of the circuit, large glitches in form of impulses are observed at the output terminal. This problem is addressed using better switch. This structure also offers a merit in form of less no. of transistors as well. 4-bit binary weighted current steering DAC is as shown in Figure 4

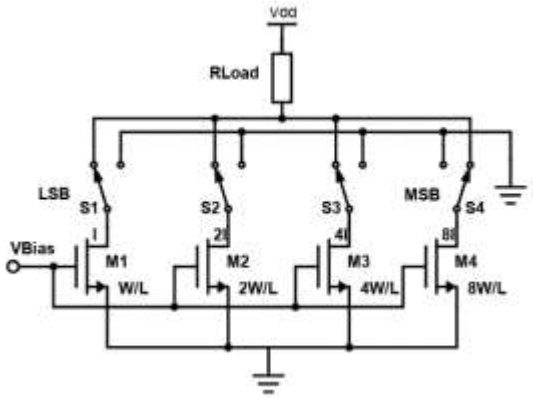

Figure 4 4 bit binary weighted current steering DAC

The present work is focused to provide following merits over the existing designs reported in last decade. The design objective is to minimize DNL and INL without too much compromising power consumption and chip area for the application in Bio medical field. After carrying out thorough literature survey, simulations and analysis, following modifications are done to bring novelty in proposed DAC

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For the proposed design and simulation, cadence tool is used with 180 nm CMOS technology. The proposed current steering DAC offers desired INL and DNL with rated power consumption.

VARIOUS SWITCHING APPROACHES

A main source of nonlinearity originates because of glitches in the current cell. More no. of transitions results more no. of changes the states of switches say on to off or vice versa. In case of 4-bit binary weighted DAC, when input changes from 0011 to 0100, big glitch is observed because of 3 transitions. Similarly when input changes from 0111 to 1000, even big glitch will be there because of 4 transitions. In case of unary weighted DAC, there is only 1-bit transition so there is no glitch but it needs more no. of current sources; for 4-bit unary current steering DAC, 15 current sources of having same value are required. Thermometer code is used to control the switches. Additional hardware is required to convert binary code into thermometer codes.

Characteristics of switch also play an important role there are various options for the same: NMOS, PMOS, Transmission gates

One of the crucial parameters for DAC is Dynamic Non linearity which includes DNL and INL.

Differential nonlinearity (acronym DNL) represents a deviation of actual step size with reference to ideal step size, where step size is a difference of analog outputs for adjacent input values.

Mathematically DNL for DAC is represented as follow:

$$DNL(i) = \frac{V_{out}(i+1) - V_{out}(i)}{ideal\ LSB\ step\ width} - 1$$

Integral nonlinearity **(**acronym INL) represents a deviation of actual analog output of DAC with reference to expected ideal value for given digital input value. It is also expressed in terms of DNL also. It is as follow

$INL\ (n) = \sum_{k=0}^{n} DNL(k)$

SIMULATION RESULTS AND DISCUSSIONS

The proposed 4-bit segmented current steering DAC is implemented using cadence virtuoso in CMOS 180 nm technology. This converter developed and simulated in a 180 nm CMOS technoogy with supply voltage of 1.8 V. and the maximum sample rate was 200 MHz under simulation. DNL and INL for proposed DAC were observed as ±0.42 LSB and ±0.4LSB, respectively. With the operating frequency of 200 Mhz, simulated power consumption was 20 mW.

Figure 5 to Figure 10 shows the simulated results and output of proposed segmented DAC using various kinds of switches say NMOS, PMOS and transmission gate.

Authors represented and compared three architectures and their outputs in form of currents.

Each architecture having two parts: one is current mirror and second is switching elements, current mirror part is common in all three architectures

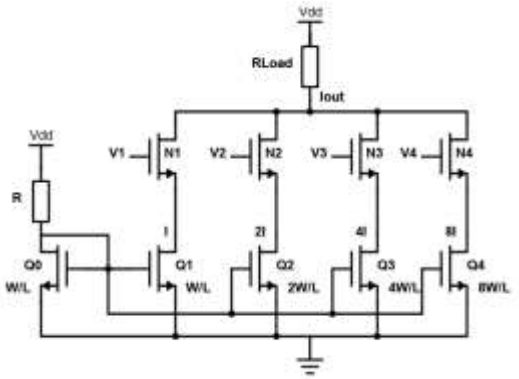

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Figure 5 Architecture of binary weighted DAC with NMOS switches

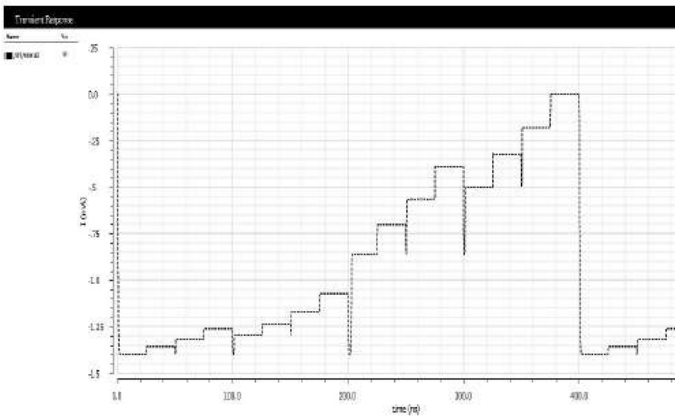

Figure 6 Current output of binary weighted DAC with NMOS switches

In case of NMOS switch based architecture, big glitches have observed and same results poor non linearity. Glitches are available when there are more number of transitions in digital inputs e.g when input change from 0111 to 1000, prominent glitch is there. The step size should be equal but it is observed that even in some cases of input changes, it is reduced rather than to be increased. Same will have adverse impact on non-linearity error in terms of INL as well as DNL.

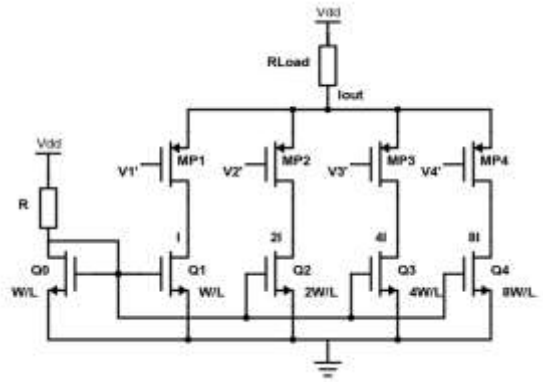

Figure 7 Architecture of binary weighted DAC with PMOS switches

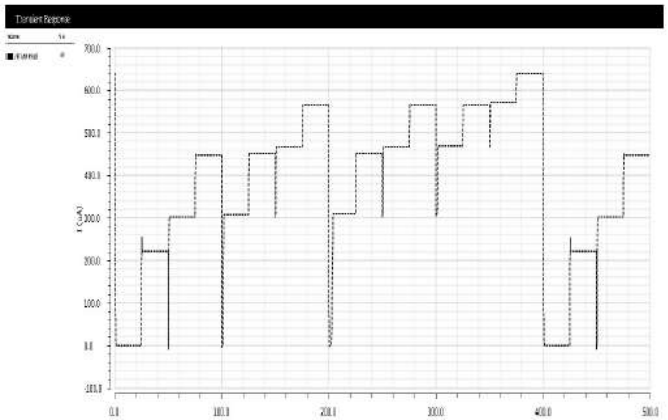

Figure 8 Current output of binary weighted DAC with PMOS switches

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Here in case of PMOS switch, same kind of observations are there as observed in case of NMOS switches. As digital input increase, output should increase. It is not always observed in case of NMOS and PMOS kinds of switches.

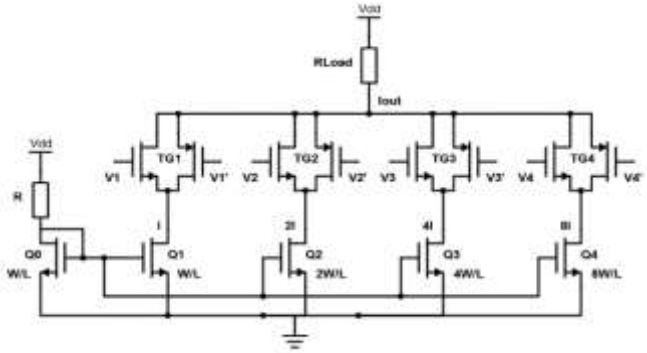

Figure 9 Architecture of binary weighted DAC with Transmission Gate switches

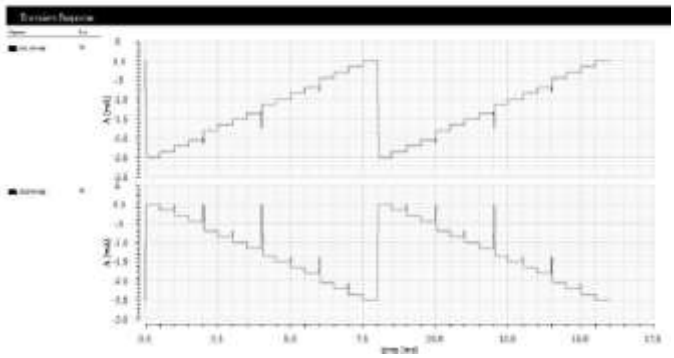

Figure 10 Current output of binary weighted DAC with Transmission Gate switches

Transmission gate is one good option as a switch. Architecture having transmission gate offers a big advantage in form of reduction of glitches as well as continuous rise of current as desired which makes lesser value of INL and DNL. Hence in proposed Current steering DAC, Transmission gate is used a switching element.
The specifications of proposed DAC are as below:

Table 1 Specifications of proposed DAC

Parameters	Proposed value
Technology	180
Resolution	4 bit
Approach	Binary weighted
Supply voltage	1.8 V
INL (Max)	0.34 LSB
DNL (Max)	0.38 LSB
Power (Max)	22mW
Frequency	200 Mhz

CONCLUSIONS

A binary weighted 4-bit current-mode digital to Analog converter (DAC) Suitable for neural stimulator based artificial retinal prostheses is designed and simulated using 180nm CMOS Process. In this implementation the authors have calculated INL, DNL with the help of PMOS switch and Transmission Gate. Based on comparison,

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Transmission gate offers better performance in form of INL and DNL. In case of Transmission Gate switch based DAC, DNL and INL are 0.38 LSB and 0.34 LSB respectively. Power consumption is observed as 22mW.

REFERENCES

1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata Mac Graw Hill, 2013.
2. R. Jacob Baker, Harry W. Li and David E. Boyce, "CMOS Circuit Design, Layout, and Simulation", IEEE Press, 1998.
3. Philip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design" Oxford University Press, 2012.
4. Seok, Changho, et al. "A 16-channel neural stimulator IC with DAC sharing scheme for artificial retinal prostheses." JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE 14.5 (2014): 658-665.
5. Rahman, Md Tanvir, and Torsten Lehmann. "A self-calibrated cryogenic current cell for 4.2 K current steering D/A converters." IEEE Transactions on Circuits and Systems II: Express Briefs 64.10 (2016): 1152-1156.
6. Mukhopadhyay, Ishita, et al. "Dual-calibration technique for improving static linearity of thermometer DACs for I/O." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 24.3 (2015): 1050-1058.
7. Sarkar, Santanu, and Swapna Banerjee. "An 8-bit low power DAC with re-used distributed binary cells architecture for reconfigurable transmitters." Microelectronics Journal 45.6 (2014): 666-677.
8. Liu, Renzhi, and Larry Pileggi. "Low-overhead self-healing methodology for current matching in current-steering DAC." IEEE Transactions on Circuits and Systems II: Express Briefs 62.7 (2015): 651-655.
9. Pal, Neelanjana, et al. "Placement-based nonlinearity reduction technique for differential current-steering DAC." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 24.1 (2015): 233-242.
10. Park, Geunyeong, and Minkyu Song. "A CMOS current-steering D/A converter with full-swing output voltage and a quaternary driver." IEEE Transactions on Circuits and Systems II: Express Briefs 62.5 (2014): 441-445.
11. Sarkar, Santanu, and Swapna Banerjee. "A 10-bit 500 MSPS Segmented DAC with Optimized Current Sources to Avoid Mismatch Effect." 2015 IEEE Computer Society Annual Symposium on VLSI. IEEE, 2015.
12. Przyborowski, Dominik, and Marek Idzik. "A 10-bit low-power small-area high-swing CMOS DAC." IEEE Transactions on Nuclear Science 57.1 (2010): 292-299.
13. Jayesh Patel, Amisha Naik. "Comparative Study of Current steering DAC based on Implementation using various types of Switches" International Journal of Advanced Research in Engineering and Technology, 11.4 (2020):452-460.
14. Mathurkar, Piyush, and Madan Mali. "Segmented 8-bit current-steering digital to analog converter." 2015 International Conference on Pervasive Computing (ICPC). IEEE, 2015.
15. Nag, Sudip, and Nitish V. Thakor. "Implantable neurotechnologies: electrical stimulation and applications." Medical & biological engineering & computing 54.1 (2016): 63-76.
16. Famm, Kristoffer, et al. "Drug discovery: a jump-start for electroceuticals." Nature 496.7444 (2013): 159.
17. Jayesh Patel, Amisha Naik. "A Low Voltage High Speed Segmented Current Steering DAC for Neural Stimulation Application". International Journal of Recent Technology and Engineering, 2020.

ISSN: 2005-4238 IJAST