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FIVE LEVEL BOOST SWITCHED-CAPACITOR MULTILEVEL MODULE MULTILEVEL INVERTER TOPOLOGY

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ABSTRACT

In this paper five level boost switched-capacitor multilevel module multilevel inverter topology is presented (BSCMLM MLI). The proposed topology is consisting of two capacitors and single dc source for generation of five inverter output voltage. The switched-capacitor circuit boost up the voltage and balancing the capacitor voltages. This five level topology offers less switching device count with capacitor voltage balancing, it lead to reducing the conduction and switching losses of converter and increase the efficiency of converter. The analyses of switching and conduction losses of suggested topology are presented. This topology is tested with variable frequency multi carrier pulse width modulation (VFMCPWM) technique with different loading conditions are carried out in MATLAB environment.

Key words: Multilevel module MLI, boost switched-capacitor, multicarrier PWM, and modulation index

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1. INTRODUCTION

Now a day's multilevel inverters are playing significant role in medium power application and motor drive applications due to low voltage and current stresses on switches, reduced harmonics, less switching losses and low switching frequency [1]. The conventional multilevel topologies includes neutral - point clamped (NPC) based inverters; flying capacitor

(FC) based inverters, cascaded H-bridge based inverter and modular multilevel converter [2] - [5].

Multiple numbers of control strategies and capacitor voltage balancing techniques are reported in [7] - [22]. The developed multilevel topologies required large number of dc voltage sources for generating multiple number of output voltage levels in inverter output voltage. It is very difficult to provide large number of dc source for "n" level inverter operation. For this reason large number of dc sources are replaced by capacitor with one or two dc sources. These large number of capacitor voltages are not balancing in inverter operation for getting desire output voltage. So, for balancing the large number of capacitor voltages, it requires technique or method for balancing capacitor voltages. The presented capacitor voltage - balancing schemes are primarily focused on diode clamped inverters [7] - [13]. Now days all the industries using NPC topology over two voltage source inverter for high power applications. This topology offered three methods to control the fundamental voltage which is generated by three level inverter. These schemes are: carrier based pulse width modulation (CBPWM) technique, selective harmonic elimination (SHE) technique and space vector modulation (SVPWM) technique. The disadvantage of NPC is unequal voltage distribution among the series connected capacitor that results unbalancing the dc link voltage. Several techniques were introduced such as dc - link neutral - point voltage stability by using equivalent sates, by using voltage feedback control and by using dc feedback current sign detection.

Flying capacitor inverter are reported in [14] - [19]. For clamping voltage, FC multilevel inverters are uses flying capacitor. These inverters offered transformer less operation and maintain an equivalent stress on switching devices. The main drawback of these converters are it required large number of storage capacitors for higher voltage steps generation. The CHB inverter is better choice for generating higher steps in inverter output voltage but it requires large number of isolated dc sources which makes the inverter complex and costly. Modular inverters are presented in [20] - [22]. These techniques are not applied for MLM-MLI. This is because of different topology structures. Space vector control technique is presented in [6] for controlling the output voltage and balancing the capacitor voltages in nested neutral point clamped (NNPC) inverter. This inverter topology is extinction of neutral point clamped inverter topology which balancing the capacitor voltage by nested neutral point but the device count compared to advanced multilevel inverter are more.

In paper a new multilevel module multilevel inverter topology is discussed. This topology is obtained from MLM-MLI. The main differences between two topologies are: in new MLM-MLI topology H-bridge is completely eliminated and instead of H-bridge, only two switches are used for polarity generation.

Section-II elaborates the operation of proposed MLM-MLI topology with switching states. Five-level boost switched-capacitor MLM topology with switching state diagrams explained in section-III. Section-IV contains analytical analysis of converter like calculation of capacitor, switching and conduction losses of converter and efficiency. Control strategy of BSC MLM is covered in section-V. Simulation results and discussions are reported in section-VI. Conclusion and references are presented in section-VII and section-VIII.

2. STRUCTURE OF PROPOSED MLM TOPOLOGY

Proposed topology is known as a new multilevel module (MLM) multilevel inverter topology with reduced switch count [23]. Proposed MLM presents reduced switches compared to existing MLM [24]. Existing MLM consist of four unidirectional blocking and bidirectional conducting (UBBC) switches for polarity generation in the form of cascaded H bridge and remaining all switches are bidirectional blocking and bidirectional conducting (BBBC)

switches which are used for generating DC voltage levels in converter output voltage. In proposed topology Cascaded H Bridge (four switches) is completely eliminated which are used for polarity generation and two switches are used for polarity generation in suggested topology.

In this paper five level MLM topology is configured. It required five switches for generating five level output voltage. In five switches, four switches are UBBC and one switch is BBBC. Suggested topology with five level output voltage is shown in fig. 1. S1 switch is used for positive polarity generation and S4 switch is used for negative polarity generation. Switches S2, S3 and S5 are used for generating the dc levels in converter output voltage. Switches S1 and S4 are also used for generating zero voltage level. In proposed topology two switches are conducting for generation of each dc level in converter output voltage where as in existing topology, three switches are conducting for generation of each dc level in converter output voltage. The configured five level MLM topology switching states are shown in table. 1.

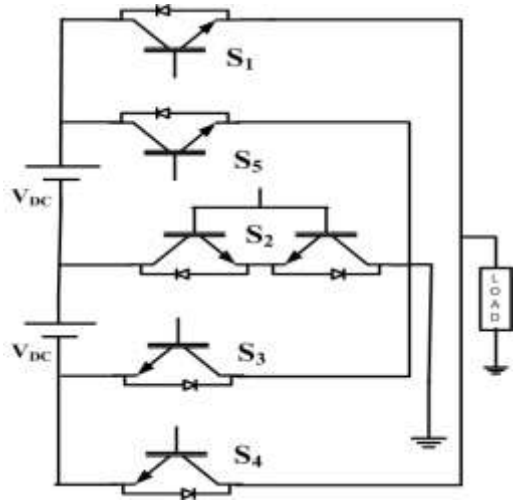

Figure 1 Proposed Five-Level MLM Topology

Table 1 Switching states of five level MLM topology

State	Output Voltage	Active Switches
1	$+V_{DC}$	S_1 , S_2
2	$+2V_{DC}$	S_1 , S_3
3	$- V_{DC}$	S_2 , S_4
4	$- 2V_{DC}$	S_5 , S_4
5	0	S_1 , S_5
6	0	S_3 , S_4

3. FIVE LEVEL BOOST SWITCHED - CAPACITOR MLM TOPOLOGY

Five-level boost switched-capacitor (BSC) MLM topology is shown in fig. 2. In multilevel inverter, for increasing number of level, it required “n” number of voltage sources and it difficult to arrange the huge number of voltages to generating “n” level of output voltage. So alternative arrangement should be voltage sources are replaced by capacitors. If large numbers of capacitors are placed instead of voltage source then there is problem of capacitor balancing. The suggested five-level boost switched-capacitor MLM topology is balancing the capacitor voltages as well as boost up the inverter output voltage. The proposed five level circuit consist of two capacitors, seven switches and one dc voltage source. Switches S_6 and S_7 are used for

boost up the voltage. Switching states of five level boost switched capacitor MLM topology is shown in table. 2.

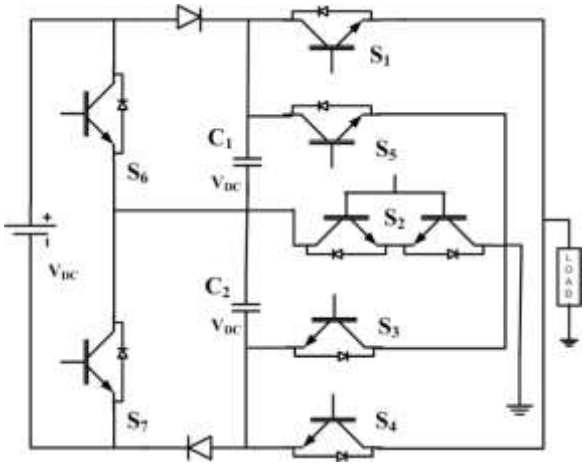

Figure 1 Proposed Five-Level BSC MLM Topology

Table 2 Switching States of Five Level BSC MLM Topology

State	Output Voltage	Active Switches	Status of Capacitor C_1 and C_2
1	$+V_{DC}$	S_1 , S_2, S_6	C_1 discharging to load and C_2 charging to DC Source
2	$+2V_{DC}$	S_1 , S_3	Both C_1 and C_2 are discharging to load
3	$- V_{DC}$	S_2 , S_4, S_7	C_2 discharging to load and C_1 charging to DC Source
4	$- 2V_{DC}$	S_5 , S_4	Both C_1 and C_2 are discharging to load
5	0	S_1 , S_5 or S_3 , S_4	--------

Suggested BSC MLM topology is consist of five switching states which are shown in fig. 3.

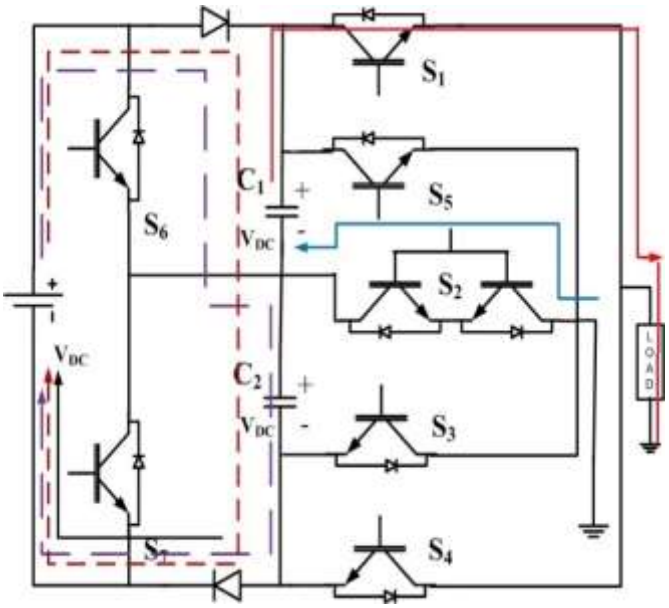

Figure 2 (a) Generation of $+V_{DC}$ Output Voltage

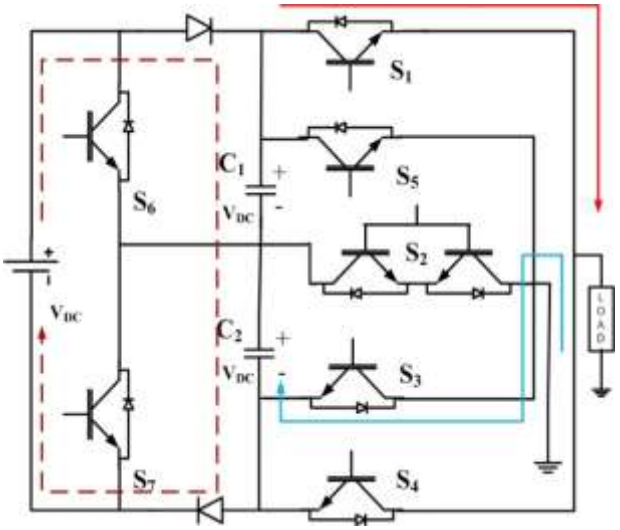

Figure 3 (b) Generation of +2 V_{DC} Output Voltage

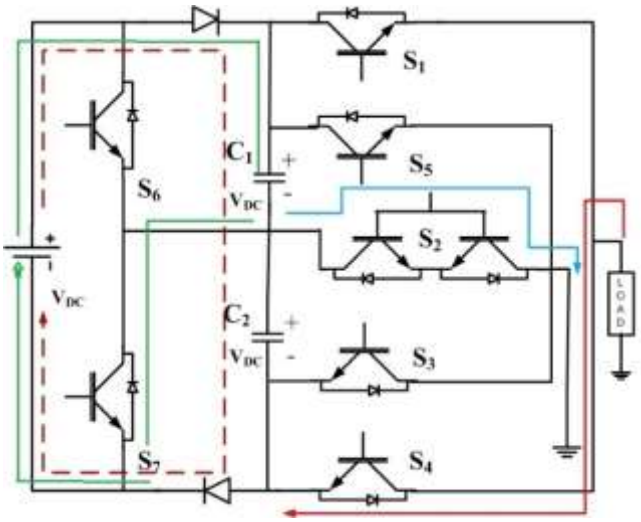

Figure 4 (c) Generation of - V_{DC} Output Voltage

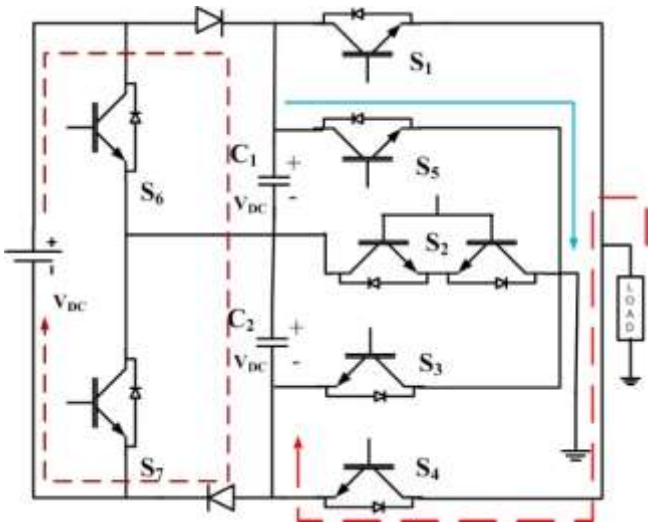

Figure 5 (d) Generation of -2 V_{DC} Output Voltage

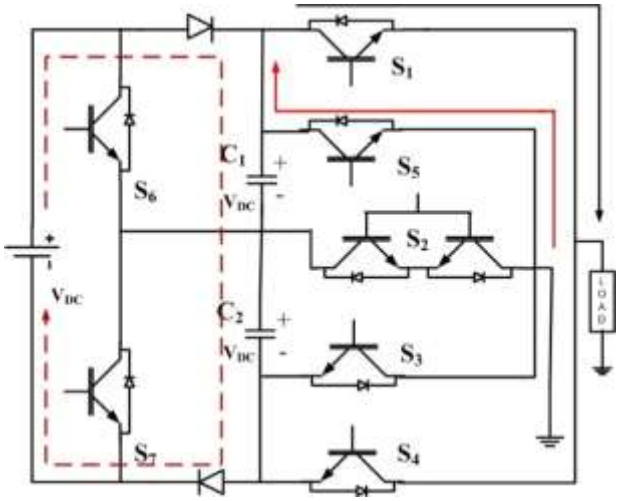

Figure 6 (e) Generation of "0" Output Voltage

4. ANALATICAL ANALYSIS

4.1. Calculation of Capacitor:

In this section, value of capacitor calculation and efficiency of converter are presented. In proposed topology, capacitor is charged to dc source through diode or switch.

So, total equivalent resistance of charging pach is R_{ch}. R_{ch} is series combination of capacitor series resistance (R_{ESR}), IGBT on state resistance (R_{on}) and resistance of diode (R_D). Equivalent resistance of switch represents the switching losses of the IGBT.

Hence, capacitor voltage (*VC*) and current (*IC*) are calculated as follows:

$$\boldsymbol{V_c(t) = (V_{dc} - V_{c_{min}})(1 - e^{\frac{-t}{R_{ch}t}}) + V_{c_{min}}} \quad (1)$$

$$\boldsymbol{V_{R_{ch}} = V_{dc} - V_c(t)} \quad (2)$$

$$\boldsymbol{I_c(t) = \frac{V_{dc} - V_{c_{min}}}{R_{ch}} e^{\frac{-t}{R_{ch}C}}} \quad (3)$$

Where,

$V_{c_{min}}$ = Capacitor initial voltage in every charging process

$(V_{c_{max}})$ = Capacitor final voltage in every charging process and "t" is charging time period.

The maximum ripple voltage for each capacitor happens during the largest discharging time. In this time, the capacitor stored energy is pushed to load in a cycle. As the load is taken as resistive load, the continuous discharging amount of capacitor '*C'* can be obtained as:

$$Q = \int_{t_a}^{t_b} I_{Load} \sin \omega t dt \quad (4)$$

Thus, the capacitance of capacitor 'C' should gain

$$C > \frac{Q}{\Delta V_{ripple}} \quad (5)$$

ΔVripple = an acceptable voltage ripple over the capacitors that should be 5% - 10%,

ILoad = the amplitude of the load current and

(*ta-tb*) = largest discharging time

B. Efficiency Calculation:

The efficiency can be simply calculated by:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{ou}+P_{loss}} \times 100 \quad (6)$$

$$= \frac{\frac{V^2_{out(rms)}}{R_{Load}}}{\frac{V^2_{out(rms)}}{R_{Load}}+P_{sw}+P_{cond}} \times 100 \quad (7)$$

Here, The power losses (Ploss) = the switching losses (Psw) + Conduction losses (Pcond).

So, the switching losses are defined as:

$$P_{sw} = f(\sum_{i=1}^{N_{sw}}(\sum_{j=1}^{N_{on(i)}} E_{on(ij)} + \sum_{j=1}^{N_{off(i)}} E_{off(ij)})) \quad (8)$$

Where,

f = the fundamental frequency

Nsw = the number of switches

Non(i) and Noff(i) = number of turning on and off of the ith switch during a period.

Eon(i) and Eoff(i) = turning on and off energy losses for ith switch.

Conduction losses (Pcond) for switches and diodes are obtained from the equations shown below:

$$P_{cond(sw)} = \sum_{i=1}^{N_{sw}}(V_{on(sw_i)} \times I_{ave(sw_i)} + R_{on(sw_i)} \times i^2_{rma(sw_i)}) \quad (9)$$

$$P_{cond(D)} = \sum_{i=1}^{N_D}(V_{on(D_i)} \times I_{ave(D_i)} + R_{on(D_i)} \times i^2_{rma(D_i)}) \quad (10)$$

Where, $V_{on(sw_i)}$ and $V_{on(D_i)}$ are on - state voltages of i^{th} switch and diode. $R_{on(sw_i)}$ and $R_{on(D_i)}$ are internal on - state resistances of i^{th} switch and corresponding diode.

5. CONTROL STRATEGY

To normalize the inverter output voltage and plummeting the harmonic gratified in inverter output voltage, it must select the most suitable PWM method. In proposed BSC MLM topology multi carrier sinusoidal PWM (SPWM) technique is functional to the switching devices, in which fundamental frequency of sinusoidal wave modulated with high frequency of triangular carrier wave(s). The generating DC level in inverter output Voltage is based on multi carrier PWM technique. Frequency and amplitude of the multiple carrier signals are diverse constructed on the PWM method. Amplitude of modulation index is the ratio of peak magnitude of reference sinusoidal wave to peak amplitude of high rate of recurrence carrier wave. Rate of recurrence modulation index is distinct as the ratio of carrier wave frequency to reference sinusoidal wave frequency. Notation of Amplitude modulation index and rate of recurrence modulation index are set by Eqn. (1) and (2) correspondingly.

$$M_A = \frac{A_m}{A_c} \quad (11)$$

$$M_F = \frac{F_c}{F_m} \quad (12)$$

Variable frequency multi carrier (VFMC) PWM method is conferred in proposed topology. In this method, M_A is continued at 0.875 and M_F is at 80. The fundamental component of the inverter output voltage is detected by MATLAB simulation environment. In VFMC PWM, bipolar multi carter PWM technique is used. In bipolar multi carrier PWM method, "N-1" high frequency carrier waves are used for "N" numeral of voltage levels.

5.1. Variable Frequency Multi Carrier PWM Method

In this multi carrier PWM method, equal amplitude of one volt and frequency of 2 kHz, 4 kHz are assigned to high frequency carrier waves. Low (2 kHz) frequency is assigned to uppermost carrier wave and high frequency (4 kHz) assigned to lower most carrier wave. These high frequency triangular waves are associated with fundamental frequency reference sine wave which is shown in Fig. 4.

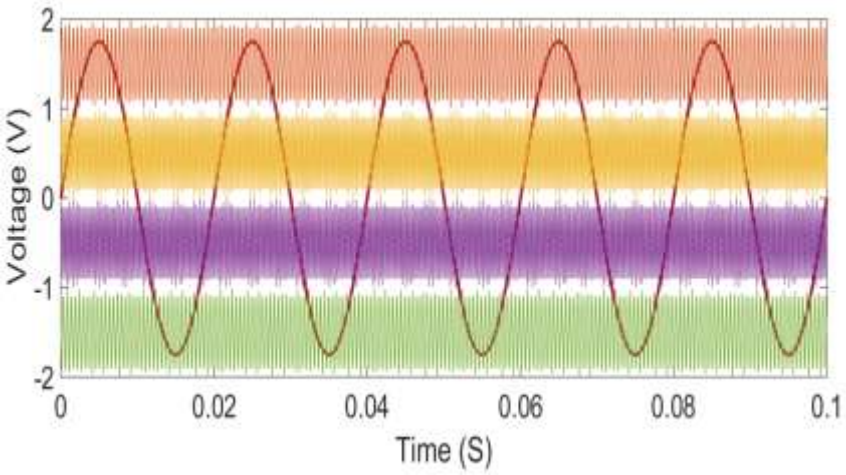

Figure 4 Variable frequency Multicarrier PWM Method

(X-Axis: 0.01 Sec/Div and Y-Axis: 0.5 Volt/Div)

6. SIMULATION RESULTS AND DISCUSSIONS

Variable frequency multi-carrier PWM function to the suggested boost switched-capacitor multilevel module multilevel inverter structure has been presented. The significance of M_A is continued at 0.875 and significance of M_F is sustained at 80. The topology constraints involved in Simulink model:

DC Voltage = 100 V

Capacitor (C_1, C_2) = 470 µF

Carrier Frequencies = 2 kHz, 4 kHz

Resistive load R = 100 Ω

Resistive and Inductive Loads = 100 Ω, 100 mH

Inverter phase voltage simulation is exposed in Fig. 5. In MATLAB simulation single dc voltage source is connected to inverter input terminal through boost switched-capacitor circuit.

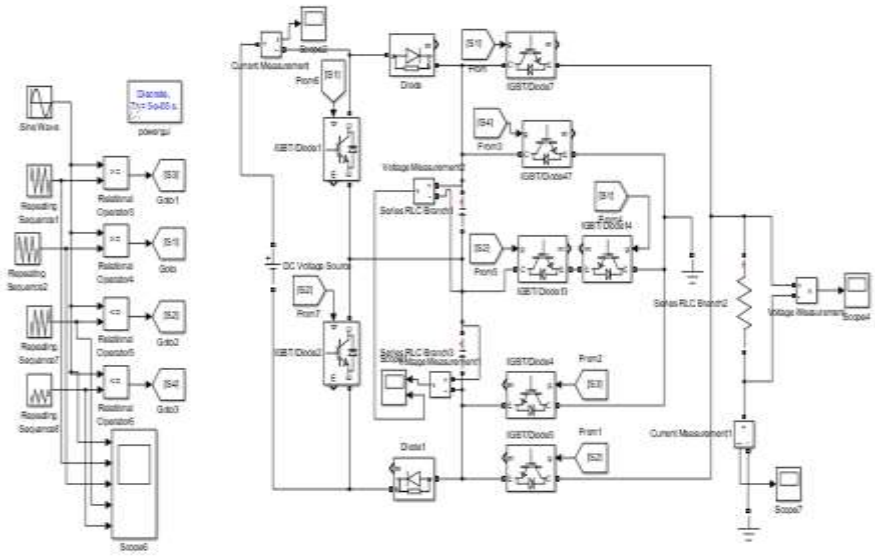

Figure 5 Simulation of BSC MLM Topology

Gate pulses and inverter output voltage are shown in figures 6 and 7.

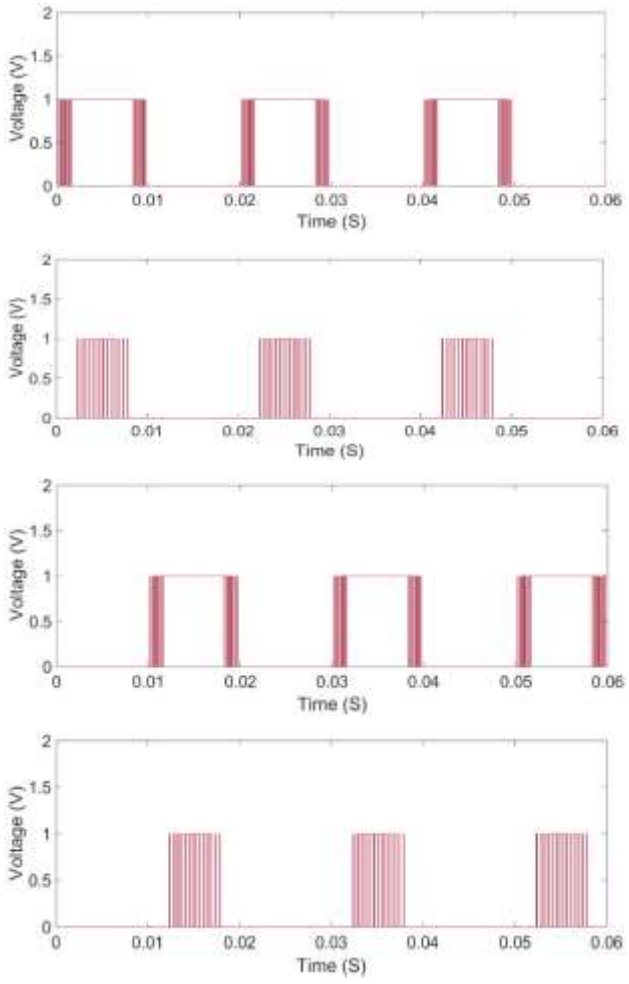

Figure 6 Gate Pulses of BSC MLM Topology

In fig. 6, the uppermost first and second gate pulses are generate the $+2V_{dc}$ and $+V_{dc}$ voltages. Lowermost first and second gate pulses are generate the $-2V_{dc}$ and $-V_{dc}$. For zero voltage level, no gate pulse is applied.

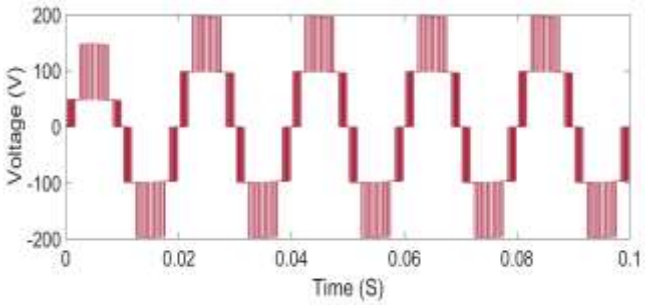

Figure 7 Five Level Inverter Output Voltage

Inverter current for R (100 Ω) load and RL (100Ω, 100 mH) load are shown in fig. 8 and fig. 9.

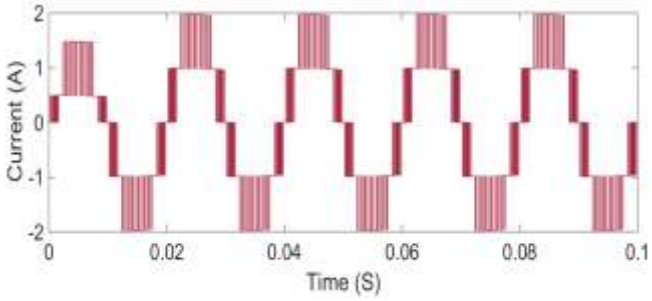

Figure 8 Inverter Current for R (100 Ω)

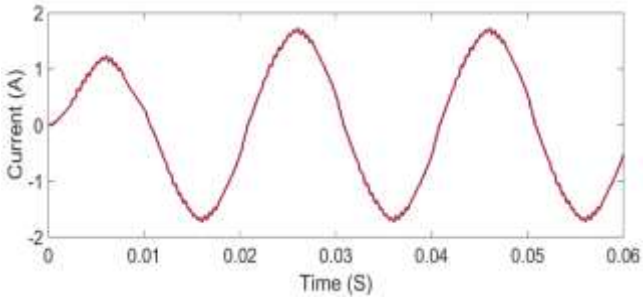

Figure 9 Inverter Current for RL Load (100 Ω, 100 mH)

Two capacitor voltages are shown in fig. 10 and 11. In simulation, applied dc source voltage is 100 V. By using boost switched capacitor circuit, dc source voltage is boost up to 200 V and the voltage balanced across the each capacitor is 100 V.

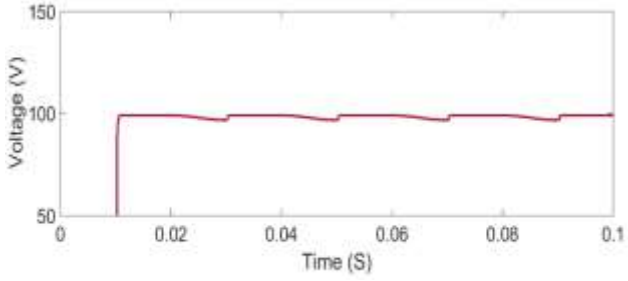

Figure 10 Capacitor C_1 Voltage

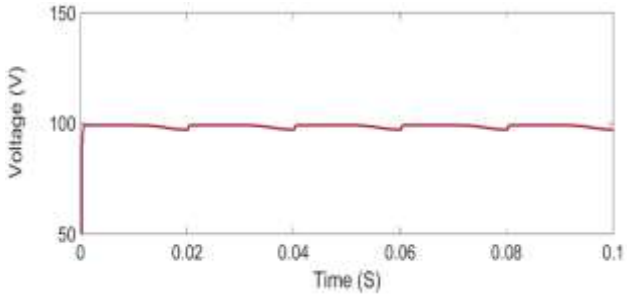

Figure 11 Capacitor C2 Voltage

Inverter line voltage and three phase voltages are shown in figure 12 and 13. For generating three voltages, in controlling circuit the reference sinewave phase angle is shifted by 120^0 for phase-Y and shifted by 240^0 for phase-B.

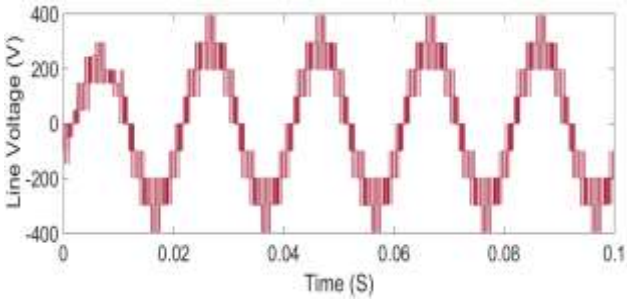

Figure 12 Inverter Line Voltage

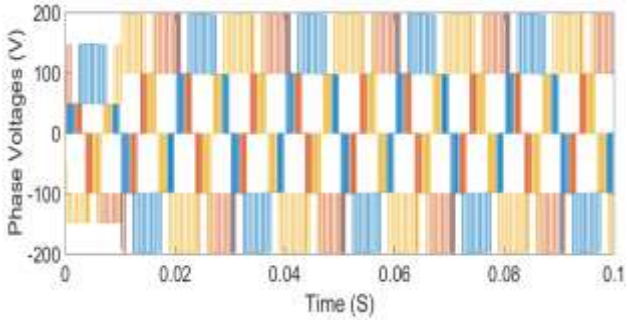

Figure 13 Inverter Three Phase Voltage

7. CONCLUSION

In this paper, a new topology of capacitor voltage balancing with boost up dc link voltage for multilevel module multilevel inverter topology is presented. The switching states of suggested topology are discussed along with switching state circuits. Analytical analysis of switching and conduction losses of BSC MLM topology is discussed. The BSC MLM topology working and operation is confirmed with MATLAB environment.

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