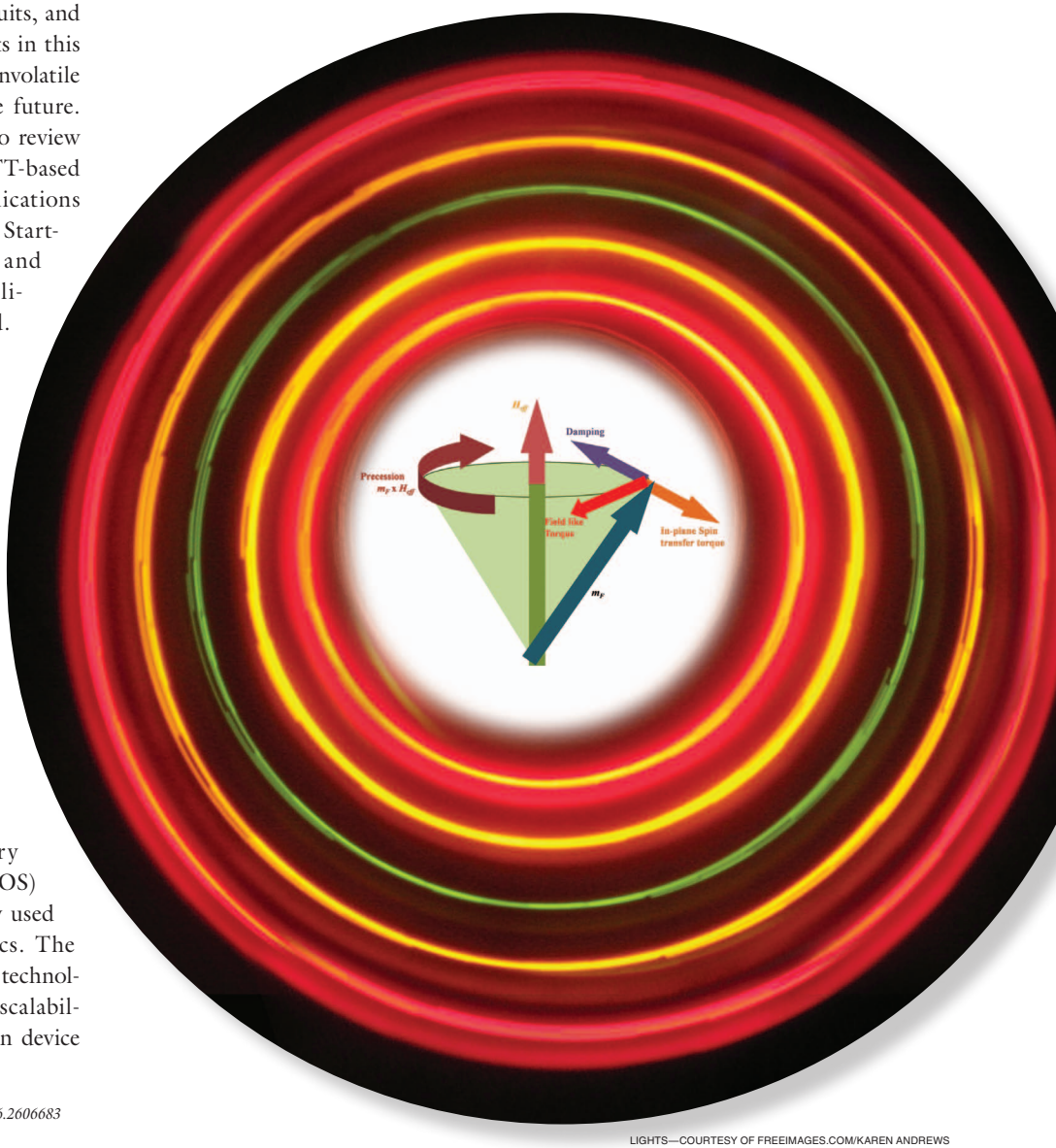
Spintronics-Based Devices to Circuits

Perspectives and challenges.

THE SCIENCE OF USING THE electron's spin in electronic devices is popularly known as *spintronics*. Researchers have been exploring spintronics to achieve nonvolatility, low dynamic power, zero standby power, and high device density. Several novel materials and phenomena have recently been discovered in this field, including the monumental spin-transfer torque (STT) effect. Since then, aggressive research activities have been conducted in both academia and industry in the field of STT-based devices, circuits, and memories. The accomplishments in this field can be revamped to a nonvolatile computing architecture for the future. The purpose of this article is to review the status and prospects of STT-based devices and their circuit implications along with future challenges. Starting with the basic concepts and device physics, advanced applications of STT are discussed. The outlook for cutting-edge technology is provided in terms of novel magnetoresistive devices embodied in the form of magnetic tunnel junctions (MTJs) controlled by the giant spin Hall effect (GSHE) and an electric field. Moreover, the concepts of all-spin logic (ASL) and MTJ-based logic are discussed. Their circuit implications and associated challenges are also reviewed.



LIGHTS—COURTESY OF FREEIMAGES.COM/KAREN ANDREWS

OVERVIEW

Over the years, complementary metal–oxide–semiconductor (CMOS) technology has been extensively used in all disciplines of electronics. The advantages of pervasive CMOS technology are directly based on its scalability. The continuous reduction in device

Digital Object Identifier 10.1109/MNANO.2016.2606683
Date of publication: 20 October 2016

SHIVAM VERMA, ANANT ARAVIND KULKARNI, AND BRAJESH KUMAR KAUSHIK

dimensions in the last few decades resulted in the improvement of CMOS device performance, that is, the reduction in dynamic power dissipation, area, and delay. However, with continuous scaling, short channel effects (like quantum mechanical tunneling, mobility degradation, hot carrier effects, drain-induced barrier lowering) and reliability problems arose. These short channel effects in conventional CMOS technology cause severe static leakage beyond the 22-nm technology node. Hence, one has to look for possible replacements for conventional CMOS technology, which has actually reached the brink of its scaling limit.

Spintronics has transpired as one of the most capable technologies in the impending post-CMOS era. The stupendous growth in spin transport devices and magnetic materials has gathered enormous interest among researchers. Spintronics technology exploits an electron's spin orientation and its associated magnetic moment as a state variable instead of a conventionally used charge in CMOS technology. The information is stored as the magnetization state of a nanomagnet instead of a charge on the capacitor [1]. Unlike a charge that depreciates due to static leakage current in conventional CMOS technology, the magnetization state can be retained almost indefinitely in spintronics-based circuits and memory. Moreover, the magnetization state can be manipulated in the low-energy budget by using the phenomenon known as STT.

Considering these developments, researchers have shifted their focus toward the development of a spintronics-based computing architecture with negligible static leakage. Hence, if most parts of a computer system are built of nonvolatile devices, the power supply to them could be turned off to avoid huge energy losses. Such architecture of computers is known as *normally off architecture*. Moreover, such architectures should possess immediate turn-on capability with full performance.

This article aims to enlighten readers about STT-based devices, circuits, and memory. Starting with basic concepts and device physics, it moves toward advanced applications of STT and provides an outlook for cutting-edge technology. The device physics, its implications on circuits, and the prospects of STT-based devices and circuits are analyzed.

BACKGROUND AND BASIC CONCEPTS

The concept of magnetic memories finds its roots in the discovery of the giant magnetoresistance (GMR) effect by two groups, led by Fert and Grünberg, back in 1988 [2], [3]. GMR was studied in a structure containing a nonmagnetic (NM) layer sandwiched between two ferromagnetic (FM) layers, also known as a *spin valve* [4]. It was shown that the FM layers structure with the magnetization state antiparallel to each other gives a higher value of resistance as compared to the one with the parallel (P) magnetization state. In such a device, GMR is defined as the normalized change in overall resistance of the sandwiched FM/NM/FM structure. GMR is expressed as

$$\text{GMR} = \frac{R_{AP} - R_P}{R_P}, \tag{1}$$

where the resistance (R_P) is low during the P magnetization state and high (R_{AP}) in the antiparallel (AP) magnetization state, as shown in Figure 1(a). The magnetization of one FM layer is kept fixed by designing the device such that the fixed layer has a high magnetic coercivity while the FM free layer has a low magnetic coercivity.

GMR was a weak phenomenon that prompted an analogous device, MTJ, with a stronger resistance change effect by the insertion of a tunnel barrier between FM layers. A resistance change effect similar to GMR was observed in MTJs and termed as *tunnel magnetoresistive* (*TMR*). The discovery of the TMR effect led to the invention of a new class of memory technology known as *magnetoresistive random access memories* (*MRAMs*), which stored data as the resistance state of an MTJ. The data stored in an MTJ is read through an n-channel metal–oxide–semiconductor (NMOS) transistor, in comparison to the MTJ resistance with the reference resistor of value $0.5 * (R_P + R_{AP})$. The MRAMs relied on the magnetic field generated by two orthogonal current-carrying metal lines, the write word line (WWL) and the bit line (BL), for writing the data, as shown in Figure 1(b). While using this mechanism, a higher field (greater than the threshold value) needs to be applied to ensure a proper write operation. The generation of a high field is energy expensive because a high current is required. Moreover, the half-selected cells adjacent to the desired cell get affected severely in an array [5].

A similar problem arises in nanomagnetic logic (NML) architectures,

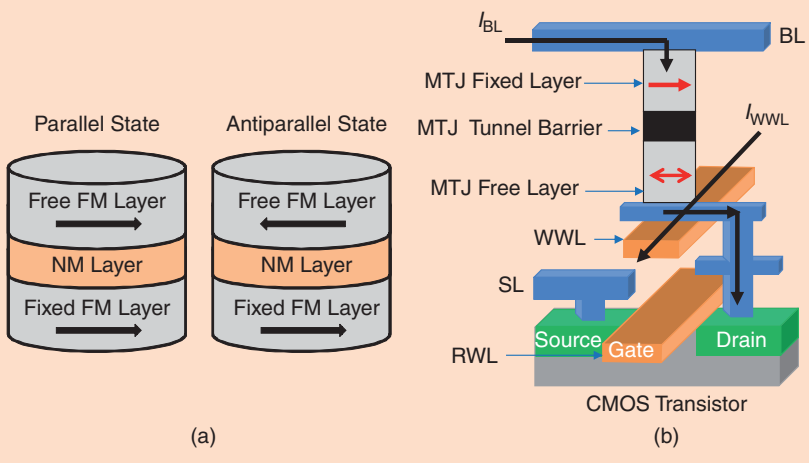


FIGURE 1 (a) The resistive states of a GMR spin valve device. (b) A field write MRAM cell with one transistor and one MTJ (1T-1MTJ cell). BL: bit line, SL: source line, WWL: write word line, and RWL: read word line.

wherein the dipolar coupling between nanomagnets is employed for logic implementation. In NML, the nanomagnets placed very close to each other serve the purpose of interconnection and propagating the logic state. These nanomagnets are susceptible to stray and high undesired dipolar interactions between successive nanomagnets that erroneously change the logic state. Hence, they lose their direction and this disturbs the flow of information.

Aforementioned concerns kept the magnetic field–based NML and memory devices away from global commercial recognition. However, the prediction of STT by J.C. Slonczewski in 1996 [6] initiated novel opportunities in this field. Achieving electrical control of magnetization, that is, STT, gave a new dimension to information processing and data storage in the last decade. This scheme of changing the magnetization orientation by a spin-polarized current proved to be much more energy efficient than the conventional use of the external magnetic field. Hence, researchers started employing STT-based magnetoresistive devices, that is, MTJs, to achieve fast and low-power memories. Moreover, novel concepts of STT-based logic circuits and ASL have been introduced recently.

MAGNETIC ANISOTROPY: SIMPLIFIED PICTURE

The bond between thin-film magnetism and spintronics is inseparable. In fact, the device-to-system-level performance in spintronics is based on minute and sensitive characteristics of thin-film nanomagnetism. One of the important characteristics of a magnetic material is its anisotropy axis or direction. The preferred direction along which a magnetic material that can be magnetized easily is known as its *easy axis* or *anisotropy direction*. This is also referred to as the *direction of minimum energy*. A pictorial view in Figure 2 provides a clearer representation. The magnetic material can achieve saturation magnetization quite easily when the magnetizing field (H) is applied along its easy axis (at 0 or 180°). Moreover, a distinct hysteretic behavior is observed while the magnetizing field (H) is parallel or antiparallel to the easy axis. On the contrary, a very high magnetizing field (H) is required for achieving magnetization close to its saturation value along the direction orthogonal to the easy axis. This orthogonal direction is known as the *hard axis* for a magnetic material.

The anisotropy behavior of a thin-film nanomagnet is considerably different from the same bulk magnetic material. In a thin-film nanomagnet, different magnetic interactions, due to its shape and the presence of adjunct interfaces, come into the picture. Anisotropy that is associated with the shape of thin-film nanomagnets is known as *shape anisotropy* or *magnetostatic energy*. In terms of field, it is popularly known as the *demagnetizing* or *magnetostatic field* that has its origin from magnetic dipole interactions. This component has the tendency to keep the magnetization of nanomagnets in the plane of the film [7], [8]. The shape anisotropy energy density (U_{dem}) is expressed as

$$U_{\text{dem}} = \frac{1}{2}\mu_0 M_S^2 \cos^2\theta, \qquad (2)$$

where μ_0 is the vacuum magnetic permeability, M_s is the saturation magnetization, and θ is the angle between magnetization and normal to the film's plane. Evidently, the shape anisotropy is minimized when magnetization lies in the film's plane. This should be the only case if the other anisotropy terms are not present in thin films, such as the interface or surface anisotropy. Hence, the effective anisotropy energy density is expressed as $U_{\text{eff}} = -K_{\text{eff}}\cos^2\theta$, where $K_{\text{eff}} = K_{\text{vol}} + (2K_s/t_{tf}) - (1/2)\mu_0 M_S^2$ is the effective uniaxial anisotropy constant. K_s is the interfacial anisotropy constant, K_{vol} is the volume anisotropy constant, and t_{tf} is the thickness of the thin-film nanomagnetic (FM) layer.

Here, the point worth noting is that the magnetization of the film is preferentially perpendicular (parallel) to the plane for $K_{\text{eff}} > 0 (K_{\text{eff}} < 0)$. This can be further understood by using the critical thickness (t_{cr}) of a nanomagnetic layer above which the nanomagnetic layer exhibits an easy axis in the plane of the film, also known as *in-plane anisotropy* (*IPA*). Evidently, below t_{cr}, the easy axis

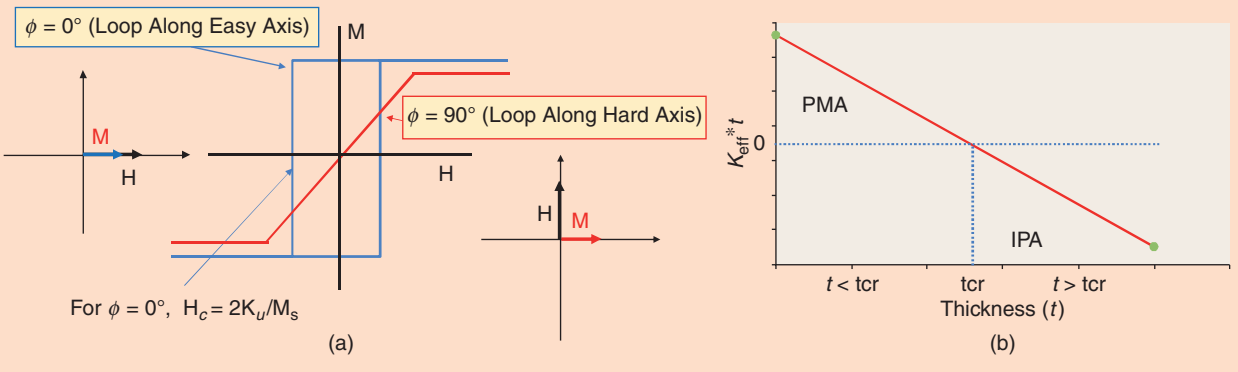


FIGURE 2 (a) The hysteresis loops along a hard and easy axis for a thin nanomagnetic layer. (b) The change in material anisotropy with thickness for a thin nanomagnetic layer.

is perpendicular to the film's plane, commonly known as *perpendicular magnetic anisotropy* (*PMA*). Figures 2(b) and 3(a) demonstrate the change in hysteretic behavior between IPA and PMA nanomagnetic FM layers. The thickness t_{cr} below which the perpendicular magnetization is energy favorable is expressed as

$$t_{cr} = -\frac{2K_s}{K_{vol} - \frac{1}{2}\mu_0 M_S^2}. \quad (3)$$

THEORY OF STT

The stupendous growth in the field of spintronics and magnetic memory was initiated in 1996, when Slonczewski theoretically predicted magnetization switching of a patterned magnetic multilayer structure by a spin-polarized current injected perpendicular to the surface area of the structure [6]. More research was stimulated by his discovery in the following years to demonstrate STT magnetization switching in multilayer structures [9]–[11]. By virtue of the STT effect, magnetization switching of a target FM layer can be achieved by a spin-polarized current generated by a reference FM layer.

The inherent capability to generate a spin-polarized current of FM materials when electrical current is passed through them forms the basis of an electrical spin injection into NM material. Owing to relatively differing densities of spin up and spin down electrons near Fermi energy, an inherent spin polarization (P) exists in FM materials. Hence, by passing electrical current through an FM/NM interface, a spin-polarized current can be injected into NM that later vanishes to zero spin polarization at equilibrium. The time required to reach this equilibrium state is known as *spin relaxation time*, while the distance up to which it exists is known as *spin relaxation/coherence length* for an NM material. Before such an equilibrium state arises, the spin-polarized current has to be employed for magnetization switching by exploiting the STT effect.

Researchers have been working with a threefold objective: first, to find an NM channel material that exhibits large spin coherence; second, to achieve tunneling-based magnetoresistive MTJ devices having a small length along the current flow; and third, to achieve large spin injection efficiency from FM to NM material. All these efforts are aimed to eventually achieve information/data manipulation by using the STT effect.

In a current perpendicular to the plane FM1/NM/FM2 multilayer structure, FM1 generates the spin-polarized current, and the magnetization direction of FM2 is free to be manipulated using STT. The magnetization dynamics of FM2 in response to STT generated by FM1 are determined from the Landau–Lifshitz–Gilbert–Slonczewski (LLGS) equation stated as follows:

$$\frac{d\vec{m}_F}{dt} = -\gamma(\vec{m}_F \times (\vec{H}_{eff} + \vec{H}_{TH})) + \alpha\left(\vec{m}_F \times \frac{d\vec{m}_F}{dt}\right) - \vec{\tau}_{ST}, \quad (4)$$

where m_F denotes the unit vector in the direction of magnetization under the influence of spin torque τ_{ST}, γ is the gyromagnetic ratio, and α is the damping constant. The effective field (H_{eff}) is determined by the vector sum of the external magnetic field, exchange field, demagnetizing field, thermally fluctuating field (H_{TH}), and anisotropy field. H_{TH} is the stochastically fluctuating field to capture the effect of random thermal noise at finite temperature. The resulting equation after augmenting H_{eff} with H_{TH} is a stochastic differential equation of the Langevin type [12].

The magnetization dynamics can be understood using Figure 3(b). In the absence of a spin-polarized current, only a precession and damping torque acts on the free layer magnetization (m_F). The torque $m_F \times H_{eff}$ provides a precessional torque on magnetization so that the tip of the magnetization vector revolves around H_{eff}. The damping torque tries to align m_F with H_{eff} and is always directed toward the center of the precession circle. As the spin-polarized current is applied, a fieldlike torque and

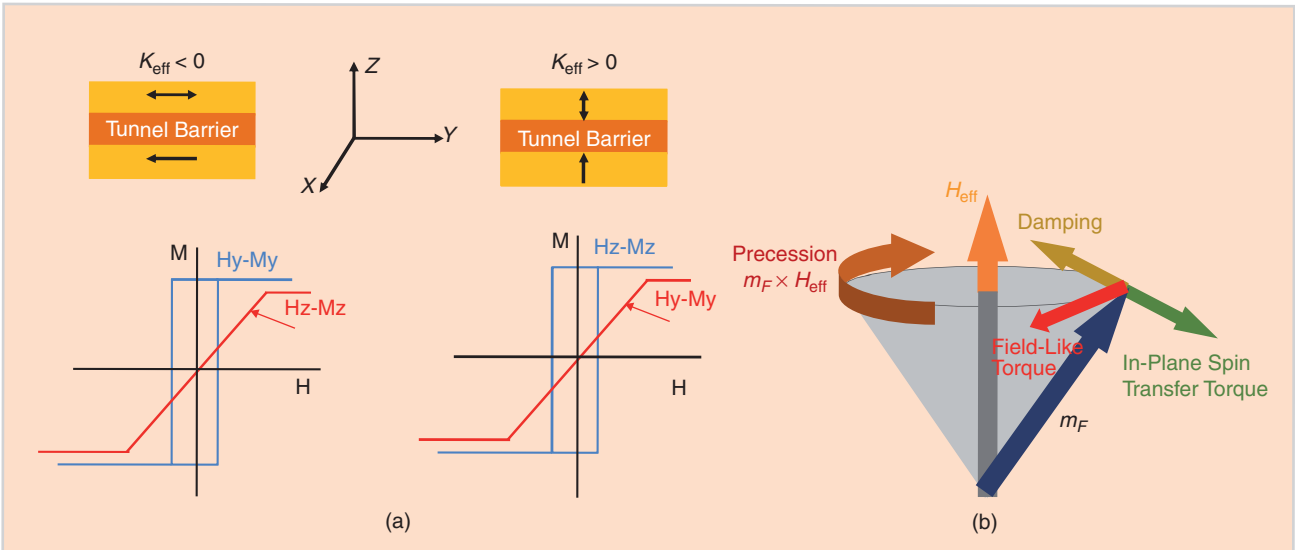


FIGURE 3 (a) The in-plane and perpendicular magnetic anisotropy. (b) The STT-based magnetization dynamics based on the LLGS equation.

in-plane Slonczewski's torque act on the magnetization, collinear, respectively, with precessional and damping torque [13]. The terms *in-plane* and *perpendicular to the plane* are considered according to the plane formed by the vectors m_F and H_{eff} [see Figure 3(b)].

It is worth noting that all these torques act only when the magnetization is displaced from its equilibrium position, away from equilibrium positions at 0 or 180° from H_{eff}. Depending on the direction of the spin-polarized current, the in-plane Slonczewski's torque aids or opposes the damping term to decide the eventual orientation of the magnetization of the FM2 (target) layer. The STT term represented by τ_{ST} in (4) is expressed as

$$\tau_{ST} = \underbrace{a_J(\vec{m}_F \times \vec{m}_F \times \vec{m}_P)}_{\text{slonczewski's}} + \underbrace{b_J(\vec{m}_F \times \vec{m}_P)}_{\text{FLT}},$$
$$a_J = \frac{\eta\gamma\hbar J}{2e\mu_0 M_F d_F},$$
$$b_J = \frac{\eta\gamma\hbar J}{2e\mu_0 M_F d_F}(b_0 + b_1 J), \qquad (5)$$

where b_J can be a linear or quadratic function of the current density (J) responsible for generating STT. The terms μ_0, $\hbar$, e, m_P, and η represent the vacuum permeability, reduced Planck's constant, electronic charge, unit vector along the spin polarization generating the STT, and STT efficiency, respectively. Furthermore, the ratio b_J/a_J is negligible for spin valves but lies between 10 and 100% for MTJs [14], [15]. Hence, while using the LLGS equation in the case of MTJs, the fieldlike torque cannot be neglected.

Researchers are working on customizing magnetization dynamics to achieve faster and low-power operation by varying the material properties and geometry. These material and geometry parameters significantly impact the out-of-plane, fieldlike STT term.

STT-BASED DEVICES

This section deals with advanced magnetoresistance-based PMA MTJs, ASL devices (ASLDs), and GSHE-based devices, all of which rely on STT switching for magnetization manipulation and data storage. The objective of all these devices is to generate a strong spin-polarized current (preferably 100%) and enable this current to strike a target FM layer (data storage layer). A novel mechanism of magnetization switching using electric field/voltage and MTJs exploiting GSHE is also discussed. This section focuses on the basic operation of STT-based devices, recent experimental results, emerging architectures, and associated challenges.

STT MTJS

As the name suggests, the MTJs are heterojunctions exploiting spin-dependent quantum-mechanical tunneling. The need to use a tunnel junction as a magnetoresistive device arose due to low sensitivity and magnetoresistance ratios obtained in the existing technology, then GMR-based spin valves. The tunnel barrier used in MTJs is an insulating oxide such as TiO_X, AlO_X, and later on MgO_X. The insertion of the tunnel barrier between FM electrodes provided a tremendously boosted TMR ratio.

The discoveries of large and consistent TMR values at room temperature in Al_2O_3-based MTJs [16] and later in high-quality epitaxial CoFeB/MgO/CoFeB MTJs [16], [17] have stimulated a surge of interest in this phenomenon. These discoveries also stimulated significant progress of magnetoresistive memories, wherein the data is stored as a resistance state. This resistance state is further governed by the relative magnetization orientation of the FM electrodes. TMR is analogous to the GMR effect in spin valves, expressed as $\text{TMR} = (R_{AP} - R_P)/R_P$, where R_{AP} and R_P are P and AP resistances of the MTJ. TMR depends strongly on the choice of the electrode, barrier materials, fabrication technique, and quality of interfaces.

An MTJ is a multilayer stacked structure with three primary entities known as the *FM free layer* (generally CoFeB), *tunnel barrier* (MgO), and FM fixed layer (CoFeB). The FM fixed layer is itself composed of three layers, namely, a synthetic antiferromagnetic (SyAF) stack with a reference layer (CoFe), a spacer layer (generally Ru), and a fixed layer (generally CoFeB). An antiferromagnetic pinning layer (generally IrMn or PtMn) is used for pinning the fixed layer with the help of an exchange field so that its magnetization orientation cannot be changed. The architecture is shown in Figure 4(a).

The device physics of an MTJ involves a combination of magnetoresistance effect, quantum tunneling effect, and STT switching effect (or hysteresis), with bias voltage and temperature dependencies. The switching between two stable states is achieved using bidirectional current, as shown in Figure 4(b). A sufficiently large current from FM1 (fixed

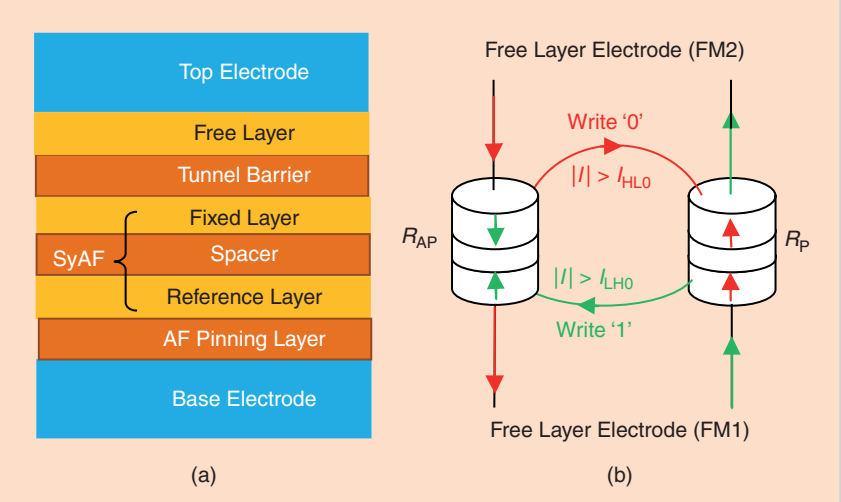


FIGURE 4 (a) The layered structure of MTJ. (b) The STT switching and operation of an MTJ.

layer) to FM2 (free layer) above a minimum threshold value (I_{HL0}) switches the resistance of the MTJ from a high value (R_{AP}) to a low value (R_P). The current in this particular direction is also termed as *parallelizing current* because it makes the final orientation of the magnetization of FM layers as parallel to each other. The value I_{HL0} is defined as the minimum current that generates sufficient antidamping torque so as to generate sustained oscillations of magnetization (m_F) about the effective field (H_{eff}) at 0 K. Similarly, an adequate antiparallelizing current from FM2 to FM1 above a minimum threshold value (I_{LH0}) switches the resistance from a high value (R_P) to a low value (R_{AP}).

In recent years, several variant MTJ architectures have been proposed to achieve a reduction in switching threshold current, as summarized in Figure 5. They include multiple polarizer layers to achieve a slight initial deviation in a free layer to enable easier and quicker STT switching. A structure [shown in Figure 5(a) and (b)] with multiple polarizer layers was proposed by Sbiaa et al. [18], wherein the reference and free layers are aligned perpendicular to the plane along with another polarizer layer aligned in the plane of the MTJ. By inserting a Cu/NM spacer between the free layer and polarizer, the STT originated due to the spin-polarized current from the polarizer will drive the free layer slightly out of its easy axis. Once the free layer is shifted away from its easy axis, it can be switched comparatively easily through the spin-polarized current generated by the fixed layer. The canted polarizer structure proposed by You [19] is shown in Figure 5(c). The author demonstrated a similar reduction in switching threshold current by using polarizer layers whose magnetization orientations were noncollinear with a reference (fixed) layer. It was estimated that switching of the free layer can either be improved or delayed depending on the angle between polarizer and free layer.

In another alternate architecture, shown in Figure 5(d), a perpendicular-to-plane polarizer and in-plane free layers are used along with a synthetic antiferromagnetic layer [20]. This arrangement of orthogonal spin torque (OST)-based MTJs exhibited a low switching threshold current and high switching speed (< 500 ps) at 0.7-V amplitude pulses. Unlike conventional MTJs, wherein the switching occurs for only one polarity (direction) of applied voltage, the OST MTJ displays both P and AP and AP to P switching with either polarity of applied voltage. However, this could be a reliability concern in memories, as it might lead to write errors, especially under the influence of thermal fluctuations.

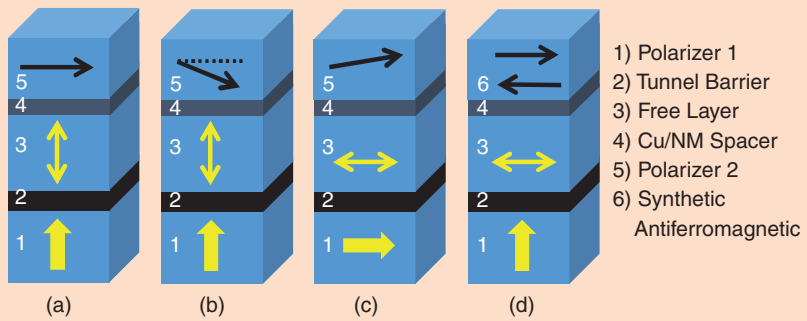


FIGURE 5 (a)–(d) The MTJ stacks with multiple polarizer layers.

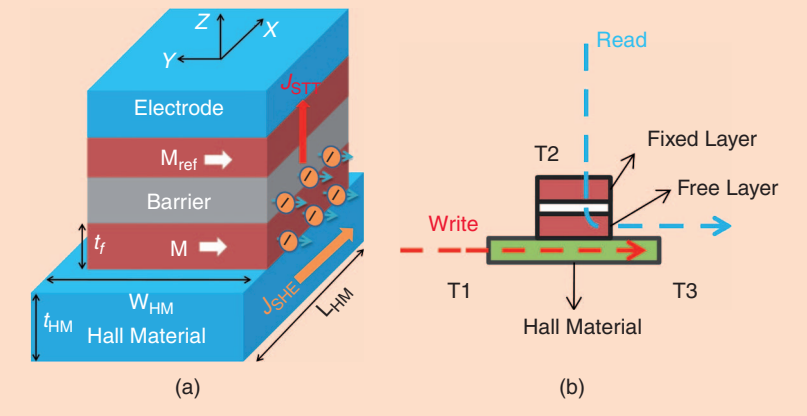


FIGURE 6 (a) The MTJ switched by GSHE. (b) The three-terminal architecture of GSHE MTJs.

GSHE-BASED MTJS

The anomalous Hall effect [21] and GSHE [22] have been known to generate a charge current from a spin-polarized current and vice versa. Although the well-known spin Hall effect was established in the 1970s [23], it could only be implemented in spintronic devices recently. These devices exploit the capability of NM material with a strong spin-orbit coupling to generate a strong spin-polarized current. The spin-polarized current is then utilized to achieve STT switching of the adjunct-free MTJ layer. The phenomenon of spin-polarized tunneling that exploited the spin filtering property of FM electrodes had an obvious disadvantage that the efficiency of a spin-polarized current could not reach 100%. However, owing to GSHE, now a pure spin-polarized current with 100% spin polarization can be achieved.

Typical architecture of a GSHE-based MTJ is shown in Figure 6(a), wherein an NM channel of a long length carries a charge current in an appropriate direction. The magnetization of the adjacent FM free layer can be switched by the generated transverse spin-polarized current. It is worth noting here that the shape anisotropy direction of the MTJ should be orthogonal to

the direction of flow of spin current to achieve STT switching.

GSHE has led to a novel three-terminal architecture of MTJs, as shown in Figure 6(b). Interestingly, these MTJ devices can now have separate read and write current paths [24], [25]. In contrast, conventional MTJs have both a spin-polarized current and charge current traveling in the same area that also involves the free/storage layer. In GSHE-based MTJs, the charge current injection area (A_{HM}) is isolated from the spin current injection area (A_{MTJ}). The spin current generated using GSHE is expressed as

$$\frac{I_s}{I_c} = \frac{A_{MTJ}}{A_{HM}} \frac{J_{STT}}{J_{SHE}} \theta_{SH}, \tag{6}$$

where I_s and I_c represent the spin current [in the z direction, as shown in Figure 6(a)] and charge current (in the x direction), respectively. J_{STT} (100% spin polarized directed toward z direction) and J_{SHE} (directed toward the x direction) are charge current densities. A_{MTJ} (A_{HM}) is surface area orthogonal to J_{STT} (J_{SHE}). It is worth noting that the direction of electron spin polarization is along the $-ve$ y direction for the generated spin-polarized current.

Interestingly, unlike conventional MTJs, the ratio of the spin-polarized current to the charge current can be greater than one. Hence, the strength of the spin-polarized current is increased while keeping the readout mechanism the same as conventional MTJs. Similar MTJs have been experimentally demonstrated using various NM materials like Ta [24], Pt [25], doped Cu [26], W [27], and topological insulators (Bi_2Se_3 and $BiSbTe_3$) [28], as the Hall channel materials have different Hall angles. The MTJs with both IPA and PMA have been achieved. The Hall angle of 0.4 for W in β-phase has been found to be the largest so far among metals. Other metals possess lower values, namely, Ta = 0.15, Pt = 0.08, and Ir-doped Cu = 0.03.

ELECTRIC-FIELD-ASSISTED SWITCHING

In the pursuit of high-efficiency magnetization switching, researchers have achieved a tremendous breakthrough that involves magnetization switching aided by an electric field. It was found that the anisotropy of thin FM layers can be tailored on the application of a voltage/electric field [29]–[31] popularly known as a *voltage-controlled magnetic anisotropy* (*VCMA*) phenomenon. The nature of this anisotropy is interfacial, hence the concept was applied to MTJs with thin CoFeB electrodes and an MgO tunnel barrier. Due to thin FM electrodes, the electric field can penetrate more effectively and overcome the shielding effect in metals. The interface anisotropy at the CoFeB/MgO interface can be lowered on the application of voltage/electric field to achieve easier magnetization switching.

In the pursuit of high-efficiency magnetization switching, researchers have achieved a tremendous breakthrough that involves magnetization switching aided by an electric field.

Wang et al. [29] exploited a biasing magnetic field and an electric field to achieve magnetization switching in $Co_{40}Fe_{40}B_{20}$-MgO-$Co_{40}Fe_{40}B_{20}$ MTJ. A unipolar/bipolar voltage of different magnitude was applied to achieve a distinguishable change in interfacial anisotropy and, hence, resistance hysteresis. The variation of interfacial anisotropy with applied electric field/voltage is determined through a linear relationship [32] expressed as

$$K_s = K_{s0} + \frac{C_s V_{bias}}{t_b}, \tag{7}$$

where C_s represents the sensitivity of interfacial anisotropy constant to the applied electric field, and t_b is the tunnel barrier thickness. Figure 7 illustrates the switching behavior in the presence of an electric field while simultaneously applying a biasing magnetic field. In the absence of an electric field, the hysteresis loop of the free MTJ layer (top CoFeB layer) exhibits a high coercivity. However, on the application of the appropriate biasing electric field, the hysteresis loop shrinks to a considerably lower width (anisotropy change of about $50\ mJm^{-2}$ [29]). Because H_{bias} is also applied, a small switching current density of the order of $10^4\ Acm^{-2}$ is sufficient to achieve the magnetization switching of the MTJ free layer. This is shown in Figure 7(b) by the black line, wherein an electric field, STT due to small current, and H_{bias} are used for magnetization switching. Of course, the direction of current required should be of favorable polarity to employ the STT effect along with the VCMA effect. Once an electric field is applied, it is also possible to switch the magnetization by using H_{bias} only. This case is shown in Figure 7(b) by a red line, wherein only the stable state is the down magnetization state.

Another more viable mechanism for utilizing electric-field-assisted MTJs to achieve high efficiency was proposed by Kanai et al. [33]. The authors employed two successive voltage pulses to achieve magnetization switching while combining the voltage/electric-field control of anisotropy (VCMA) and STT effect as shown in Figure 7(c). An external magnetic field was also applied. When the first pulse (T_{VCMA}) arrives, magnetization precession is induced due to change in magnetic anisotropy by the VCMA effect and external magnetic field. The subsequent pulse (T_{STT}) is bipolar in nature similar to conventional STT switching. The magnetization direction is switched comparatively easily using a longer second pulse.

ASLD

The concept of ASL was first proposed by Behin-Aein et al. in 2010 [1]. The device could store as well as process the information with the STT-based writing mechanism. The major advantage of this

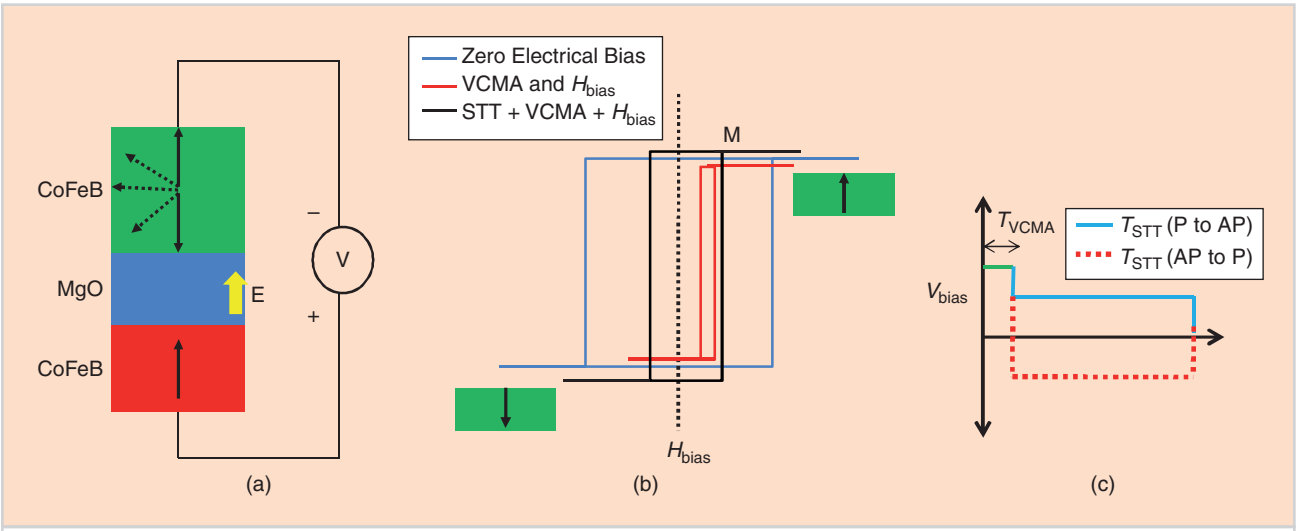


FIGURE 7 (a) The structure of VCMA MTJs. (b) The VCMA-based switching mechanism in MTJs. (c) The combined STT + VCMA switching of MTJs.

device compared to CMOS technology is the property of a self-contained logic. The ASLD consists of nanomagnets that are switched by a spin-polarized current between the stable states that represent binary information. The nanomagnets can supposedly be grown over an NM channel that carries the spin-polarized current. The structure and operation of an ASLD is shown in Figure 8.

A charge current flows from the injector FM to ground contact via a channel to produce a nonequilibrium concentration of spin-polarized electrons beneath the injector. This nonequilibrium concentration of spin-polarized electrons diffuses through the channel to reach the detector FM while undergoing some losses due to spin relaxation. The diffused electrons constitute a pure spin current (100% spin polarized) and exert STT on the detector to eventually determine its final state. The spin polarization of current through the channel depends on the potential applied to the injector FM.

Based on the polarity applied voltage, an ASLD can be operated in two modes, copy and invert, as shown in Figure 8(a) and (b). During the copy operation, a negative voltage (V) is applied to the injector. The FM injector acts as a source of majority spin electrons (spin direction along $+ve$ y axis). The spin-polarized current will diffuse through the channel and reach the detector FM. Further, the spin-polarized current will exert STT on the detector FM to finally copy the magnetization state of the injector onto the detector.

For an invert operation, a positive voltage (V) is applied to the injector. The FM injector now acts as a sink for majority spin electrons. The minority spin electrons (with spin along $-ve$ y axis) will be generated near the interface, which will diffuse through the channel toward the detector FM. The final magnetization state of the detector will be opposite to that of the injector on magnetization switching, that is, invert operation. An isolator is used to provide separation between successive conduction paths, and the ground contact is used to provide the directionality to the device. Furthermore, the tunnel barrier mitigates the conductivity mismatch and improves the spin injection efficiency. ASLDs should have the property of nonreciprocity for accurate logic operation [34], that is, the output has to be changed by the input but not vice versa.

Despite wide theoretical investigation, the proposed ASLD has so far not been transformed into fabrication. However, recently, STT switching in analogous devices has been demonstrated by

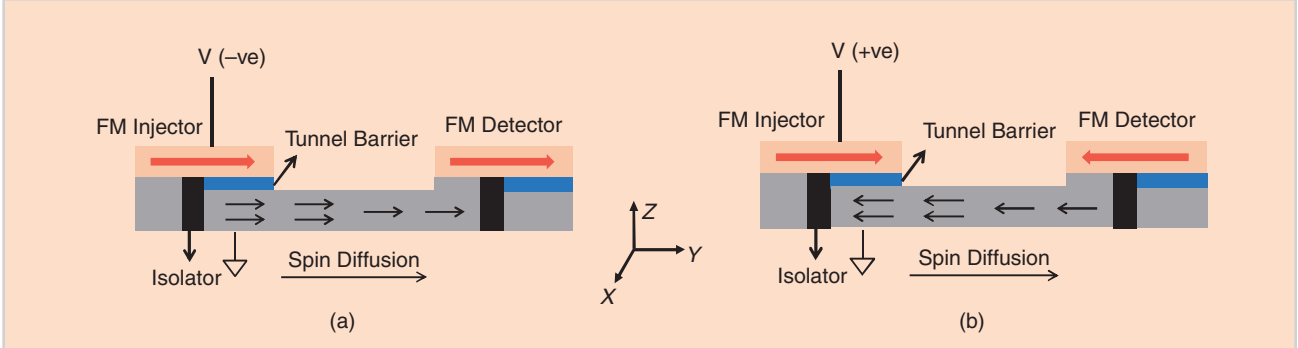


FIGURE 8 The (a) copy and (b) invert operations of an ASLD.

Lin et al. [35] using a graphene channel nonlocal spin valve. The primary challenges are to achieve a high diffusion constant and low spin relaxation so as to strengthen the spin diffusion current reaching the detector for STT switching. The fabrication of such a lateral architecture at reduced dimensions is also a critical challenge.

STT-BASED LOGIC AND MEMORY: STATUS, IMPLICATIONS, PERSPECTIVES, AND CHALLENGES

Both STT-based memory and logic are being explored vigorously by researchers. However, STT-based logic and memory offer completely different challenges. While STT-based magnetoresistive memories, STT MRAMs, are already commercialized, the implementation of logic applications is still in an elementary state. In terms of memories, researchers are extensively working to achieve efficient STT switching and high array density for embedded cache and random-access memory applications. Moreover, the goal is that the nonvolatile STT MRAMs can be accommodated universally in the memory hierarchy, from the secondary storage to the on-chip cache memory. Unlike STT MRAMs, the logic schemes proposed using STT-based devices face challenging issues including implementation and viability. However, judging by the progress of devices in this field, the circuit implications only bode well for the future. In this section, the status, implications, perspectives, and challenges will be discussed to achieve STT-based logic and memory.

STT MRAMS

STT MRAMs are a class of magnetic memories that use MTJs as a storage element. In these elements, the write operation is based on the STT mechanism, in contrast to the conventional write mechanism of using the magnetic field. In a 1-b memory cell, MTJ acts as a storage element and an NMOS transistor facilitates cell selection. The structure of an STT MRAM is shown in Figure 9(a). Their major advantages are nonvolatility, high speed, small cell size, and compatibility with CMOS technology.

In an MTJ, an interaction of spin-polarized electrons with the local magnetic moment of the FM layer takes place during which the exchange of the spin angular momentum prompts magnetization switching. For AP to P switching, the NMOS facilitates a current flow from the BL to the source line (SL), as shown in Figure 9(b). The pinned FM layer acts as a spin filter, producing a higher density of majority spin-polarized electrons. The spin-polarized electrons will sustain their spin polarization while crossing the tunnel barrier to finally exert STT on the free layer and decide its final state.

For P to AP switching, current flows from SL to BL [see Figure 9(c)], during which electrons flowing through the tunnel barrier are polarized in the direction of the free layer. On reaching the pinned layer, the electrons with spins in the direction of the pinned layer pass through, while others are reflected back to the free layer. These reflected electrons exert STT on the free layer to decide its eventual magnetization state. Because these reflected electrons are fewer in number, MTJ shows an asymmetric behavior such that the threshold switching current density for P to AP switching is larger than AP to P change. Moreover, during P to AP switching, the NMOS operates in source follower mode such that the gate to source voltage (V_{GS}) is lower than the supply voltage (V_{DD}). Low V_{GS} reduces the drive current, which is also known as *source degeneration* [36]. Hence, to reduce source degeneration and mitigate asymmetric MTJ behavior, reverse connected STT MRAM cells are used, wherein the MTJ free layer is connected to the NMOS instead of the fixed layer.

The operation of STT MRAM can be understood by reviewing Figure 10(a), which demonstrates hysteretic behavior, cell current, and read/write windows. STT MRAM write (read) operation is characterized by a write (read) margin and write (read) error rate. The write margins are defined as the difference between the write current and the switching threshold current [37]. Write error rate (WER) is the probability of failure during a particular write operation, while read disturb rate (RDR) is the probability of accidental write during a read operation. Both WER and RDR are quantified using the ubiquitous

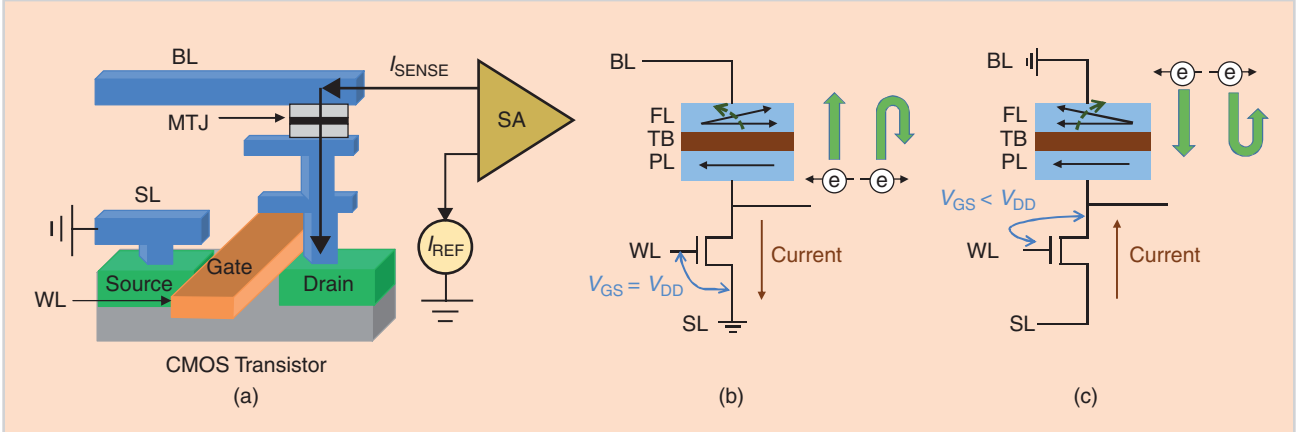


FIGURE 9 (a) The STT MRAM with MTJ integrated into CMOS technology. (b) The operation of STT MRAM cell with BL = V_{DD} and SL = 0 V. (c) The operation of STT MRAM cell with SL = V_{DD} and BL = 0 V.

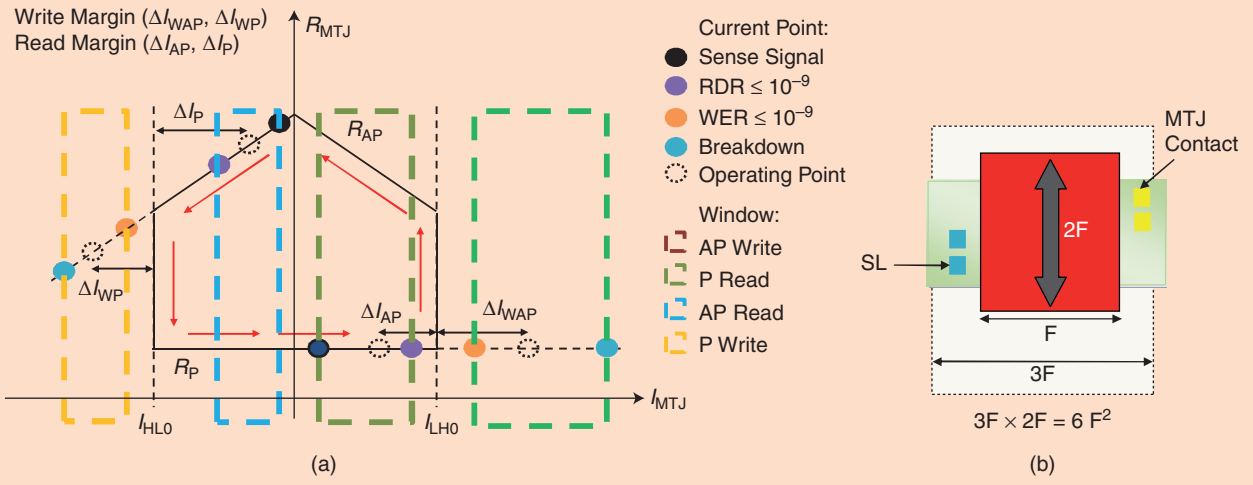


FIGURE 10 (a) A demonstration of resistance current hysteresis loop with read and write window. (b) The layout of a minimum-sized STT MRAM cell with planar CMOS technology.

formalism of stochastic STT switching of a nanomagnetic layer at a finite temperature [38]. The probability of switching at a particular current ($I_{write/read}$), whether read or write, is expressed as

$$P_{SW} = 1 - \exp\left\{-\frac{t_{PW}}{\tau_0} \times \exp\left[-\frac{E}{k_B T}\left(1 - \frac{I_{write/read}}{I_{C0}}\right)\right]\right\}, \quad (8)$$

where t_{PW} is the current pulsewidth, τ_0 is the inverse of the attempt frequency, I_{C0} is the switching threshold current (either I_{LH0} or I_{HL0}), and E/k_BT is the thermal stability factor for an MTJ. Using this expression, the WER and RDR are expressed as

$$\text{WER} = 1 - P_{SW}, \text{RDR} = P_{SW}. \quad (9)$$

WER decreases with an increase in write current above the threshold current. For reliable write (read) operation in STT MRAM, WER (RDR) should be less than 10^{-9}, which sets the minimum (maximum) allows value of write (read) current. The upper limit on write current is set by the thin dielectric layer's breakdown voltage. Further, Figure 10(b) shows the layout of a typical 1T-1MTJ STT MRAM cell with a cell size of $6F^2$. The size of the cell depends on the minimum switching threshold current. The major challenges associated with STT MRAMs are, first, switching current reduction is crucial for achieving both high memory density and reducing the overall power consumption, and, second, sustaining high thermal stability for long period data retention [39].

Starting with the seminal work by Ikeda et al. in 2010 [40], the recent experimental results of CoFeB/MgO/CoFeB PMA MTJ are shown in Table 1. Jan et al. [41] demonstrated tremendously improved results in terms of resistance-area (RA) product (6.6 $\Omega\mu m^2$), stability factor (74), and critical switching current (25 μA). In the continuity of his research, in 2014, Thomas et al. [42] demonstrated PMA MTJ stack with a high RA product (12 $\Omega\mu m^2$) and reported reduced critical switching current (29 μA), better thermal stability factor (84), and a high TMR ratio (150%).

To analyze STT MRAMs using these novel PMA MTJs, an industry standard 65-nm CMOS process design kit was used along with 60-nm PMA MTJs. The performance results are shown in Table 2. In general, the minimum size $6F^2$ has not been achievable so far with conventional IPA MTJs or PMA MTJs demonstrated till 2012. However, on using improved results from stack 2 and stack 3 shown in Table 1, the simulation results obtained in Table 2 show a considerable improvement in size with reverse connected STT MRAM cells. It can be seen that the cell size can be decreased to $9F^2$ with $F = 65$ nm while using MTJ with low RA stack 2. It is worth noting that the minimum cell size for MTJ with high RA product is quite high, hence RA product is also an important parameter in determining the minimum size of the cell for both standard and reverse connected STT MRAM cells. The reverse

TABLE 1 The recent experimental results for PMA MTJ.

RA ($\Omega\mu M^2$), REFERENCE AND YEAR	DIAMETER (NM)	TMR (%)	I_{C0} (μA)	E/K_BT	DESCRIPTION
18 [40], 2010	40	124	48	43	Stack 1
6.6 [41], 2012	40, 50, 60, 70	102	25, 45, 57, 73	74, 84, 86, 90	Stack 2
12 [42], 2014	30, 40, 50, 60, 70	150	22, 29, 62, 67, 68	77, 84, 146, 147, 150	Stack 3

TABLE 2 The STT MRAM simulation results with 65-nm CMOS process design kit.

CELL TYPE	MINIMUM WIDTH OF ACCESS TRANSISTOR (NM)	MINIMUM CELL SIZE AT F = 65 NM	WRITE MARGINS (μA) WM_P	WRITE MARGINS (μA) WM_{AP}	DESCRIPTION
Forward Connected	325	15 F^2	126	32	For low RA Stack 2
Reverse Connected	195	9 F^2	26	34	For low RA Stack 2
Forward Connected	1,000	48 F^2	163	33	For high RA Stack 3
Reverse Connected	390	18 F^2	16	98	For high RA Stack 3

connected cell offers symmetric write margins and achieves much lower cell size due to the mitigation of source degeneration or source follower phenomenon shown in Figure 9(c). However, it can be concluded that to achieve a further reduction in cell size (i.e., lower feature size), the RA product needs to be kept as small as possible while maintaining high TMR, high stability, and low threshold current. The high resistance of the MTJ at lower feature sizes so far is a serious drawback toward achieving a further reduction in power dissipation and cell size.

MTJ-BASED STATEFUL LOGIC GATES

To exploit the excellent durability and nonvolatile magnetoresistive properties of MTJs, stateful logic architectures were proposed that exploited MTJs as a memory element and for logic [43], [44]. MTJ-based logic is stateful and self-contained due to the memristive nature of MTJs, which can store logic values as well as perform logic functions. This logic scheme exploits multiple MTJ elements that can be switched at different and independent switching threshold currents for logic realizations. Separate MTJs are used as input and output MTJs, wherein a high (low) resistance state corresponds to logic 1(0).

An MTJ-based logic gate with two and three inputs is shown in Figure 11. The applied voltage (V_{supp}) decides the type of logical operation being carried out. The switching voltage corresponding to each input combination is measured to characterize the operation of the same architecture with different V_{supp}. For example, the two-input gate performs an AND operation when the magnitude of V_{supp} is chosen such that the output MTJ is switched in all input combinations except for the case when both inputs (MTJ-I1 and MTJ-I2) are in high resistance state. In other words, the switching threshold current should be higher than the obtained current when both input MTJs are in high resistance state. The preset state "logic 1" of output MTJ persists when both MTJ-I1 and MTJ-I2 are in high resistance state, resulting in an AND operation. A similar concept is used to implement a complete set of logical operations including AND, OR, NAND, NOR, IMP (implication logic), and NIMP (negative implication logic).

Table 3 shows the possible output transitions required to implement a minimal set of Boolean operations. The output MTJ is switched from its preset state only when the logic condition is satisfied. The magnitude of the supply voltage (V_{supp}) can be chosen depending on the type of operation desired from the architecture. Generally, in order that the input and output MTJs be changed independently, aspect ratios (coercivity) are varied for implementing different logical operations.

GSHE MRAMS

The drawback of STT MRAM technology is that the read and write currents follow the same path. As a result, once the threshold for write current is continuously reduced, the sense margin (the current difference between P and AP state during a read operation) is also reduced. Moreover, the thickness of tunnel barrier causes an increase in overall MTJ resistance and adversely affects the size of the access device.

It was evident from the simulated results (Tables 1 and 2) that the increase in resistance of the MTJ by two times causes an increase in width of the driver by four to five times. The GSHE-based MTJs are tailor made to overcome these drawbacks due to the decoupled nature of read and write current path. This can enable the write performance to be completely independent of the read performance. Unlike

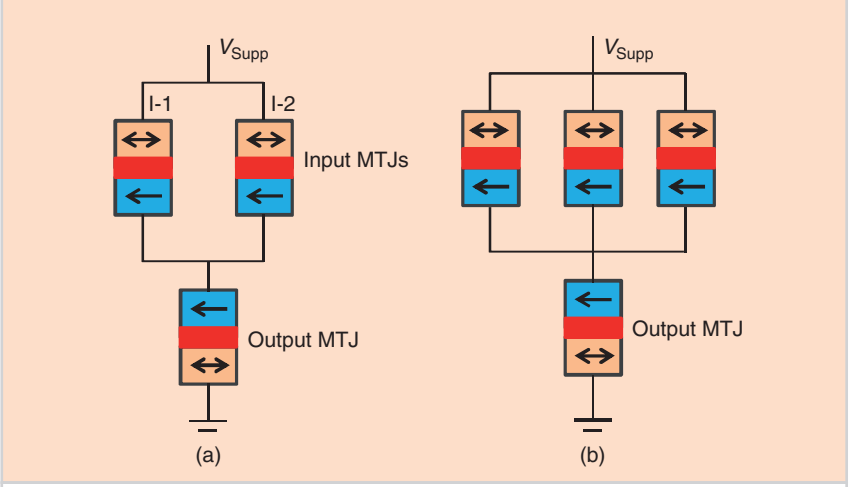


FIGURE 11 The MTJ-based logic gates with (a) two and (b) three inputs.

TABLE 3 The MTJ-based three-input logic implementation.

	LOGIC FUNCTION				
INPUT STATE	**MAJORITY**	**AND**	**OR**	**NAND**	**NOR**
Polarity of V_{supp}	Negative	Negative	Negative	Positive	Positive
Initial State of Output MTJ	1 (AP)	1 (AP)	1 (AP)	0 (P)	0 (P)
000	0 (AP to P)	0 (AP to P)	0 (AP to P)	1 (P to AP)	1 (P to AP)
001	0 (AP to P)	0 (AP to P)	1 (no switching)	1 (P to AP)	0 (no switching)
010	0 (AP to P)	0 (AP to P)	1 (no switching)	1 (P to AP)	0 (no switching)
011	1 (no switching)	0 (AP to P)	1 (no switching)	1 (P to AP)	0 (no switching)
100	0 (AP to P)	0 (AP to P)	1 (no switching)	1 (P to AP)	0 (no switching)
101	1 (no switching)	0 (AP to P)	1 (no switching)	1 (P to AP)	0 (no switching)
110	1 (no switching)	0 (AP to P)	1 (no switching)	1 (P to AP)	0 (no switching)
111	1 (no switching)	1 (no switching)	1 (no switching)	0 (no switching)	0 (no switching)

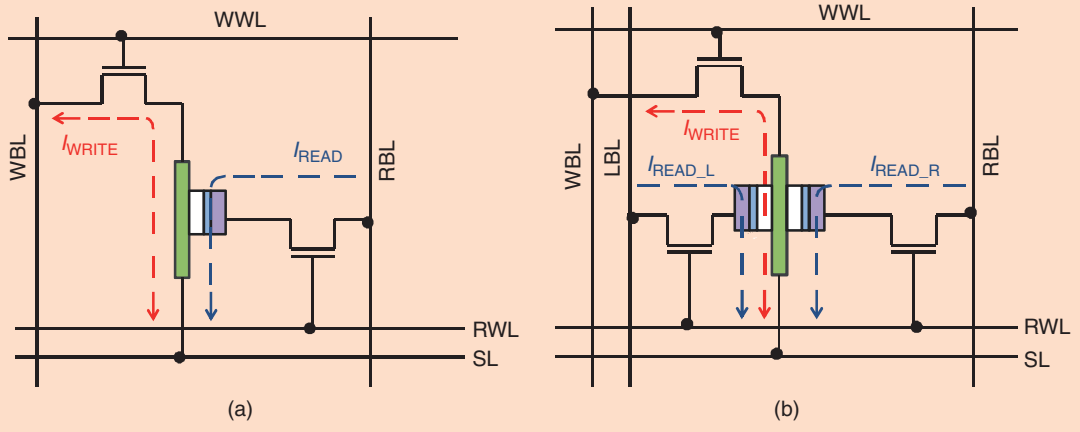


FIGURE 12 (a) The operation of a GSHE MRAM cell. (b) The operation of a differential spin Hall MRAM cell.

TABLE 4 A comparison of STT generated by SHE and SPT.

REFERENCE AND HALL MATERIAL	t_{HM} (NM)	RESISTIVITY ($\mu\Omega$-CM)	θ_{HM}	R_{HM} (Ω)	RATIO (T_{HALL}/T_{SPT})
Beta W [27]	9	210	0.4	233	3.5
Beta Ta [24]	8	190	0.15	238	1.5
Bi_2Se_3 [28]	10	1,000	0.43	1,000	3.4
Pt [25]	10	64	0.02	64	0.16

STT MRAMs, the GSHE MRAMs [45] have two bit lines and word lines.

Figure 12 shows the circuit architecture for the implementation of GSHE MRAM along with the read and write paths. Read bit line (RBL) [write bit line (WBL)] and read word line (RWL) [write word line (WWL)] are used for the read (write) operation. A level converter is also needed to generate a negative voltage at WBL required during the write 0 operation.

Another alternative architecture was proposed by Kim et al. [46] that allows a differential reading mechanism [see Figure 12(b)]. During a write operation, the write current is forced through the GSHE element to write complementary bits in left and right MTJs, whereas during differential read, the GSHE element acts as a common terminal. An appropriate read voltage is applied at RBL and left bit line (LBL). The read currents I_{READ_L} and I_{READ_R} can be compared to find out the bit stored in the cell, and no reference cell is needed.

The spin torque generated by a charge current density ($J_{C,HM}$) flowing through the Hall material (HM) and spin-polarized tunneling (SPT) can be expressed as $T_{Hall} = (\hbar\theta_{HM} J_{C,HM}\gamma/2et_f)(A_{MTJ}/A_{HM})$ and $T_{SPT} = (\hbar P J_{C,SPT}\gamma/2et_f)$, respectively. t_{HM} is the thickness of HM, t_f is the thickness of free MTJ layer, $J_{C,SPT}$ is the conventional charge current density through MTJ during spin-polarized

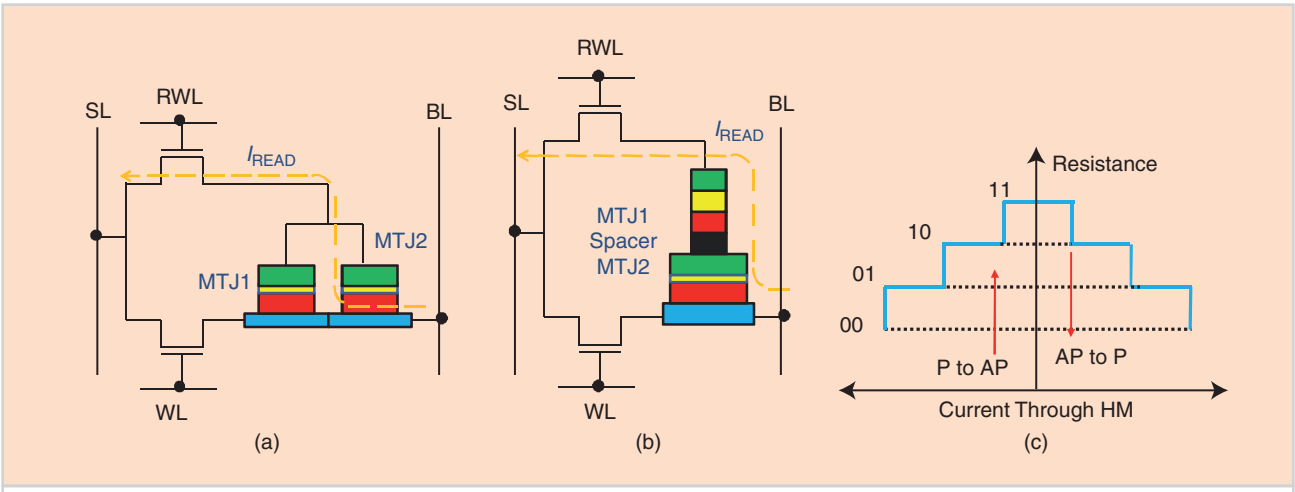


FIGURE 13 A multilevel GSHE MRAM cell: (a) a P cell and (b) a series cell. (c) The resistance hysteresis for a multilevel cell.

tunneling, θ_{HM} represents the spin Hall angle for the HM, $\hbar$ represents the reduced Planck's constant, γ is the gyromagnetic ratio, and P is the spin polarization of the current during SPT.

A simplistic comparison between the torque due to the spin-polarized current with tunneling mechanism and GSHE can be carried out by taking the ratio of the two spin torques, that is, $(T_{Hall}/T_{SPT}) = (\theta_{SH}/P)(A_{MTJ}/A_{HM})$. This ratio (placed in Table 4) is calculated for comparison using experimental data, while assuming the dimensions of HM (L_{HM} = 100 nm, W_{HM} = 100 nm, and $A_{HM} = W_{HM} * t_{HM}$) and area of elliptical STT MTJ ($A_{MTJ} = \pi/4 \times 60 \times 100\ nm^2$). The spin polarization (P) of the FM layer is assumed to be 0.6. It can be seen that the strength of STT generated by the Hall effect is quite large as compared to that generated by SPT. The strength of this torque will increase with a decrease in thickness of the HM. However, the point here worth noting is that resistance increases quite substantially as the thickness is scaled down to below 5 nm. The spin Hall angle can also be reduced with thickness. Some other drawbacks of using GSHE MTJs in memory and circuits are area overhead and complex architecture.

Another effective utilization of the high spin injection in GSHE-based MTJs is in multilevel memory cell designing [47], [48]. As a large spin-polarized current can be easily generated, simultaneous write operation on two MTJs in series or parallel is not going to be difficult. Figure 13(a) and (b) demonstrate P and series multilevel cells with write paths, while the read operation takes place through an alternate path. In this way, multiple bits can be stored in a smaller area and thereby increase the array density. Typical hysteretic behavior of resistance with respect to current in multilevel cells is shown in Figure 13(c), consisting of four resistive states and switching thresholds.

ASL DESIGN

The ASL logic circuits are based on majority function, wherein NAND (NOR) [49], [50] functions are realized with a positive (negative) supply voltage using a universal architecture shown in Figure 14. For an n-input NAND gate, $n + 1$ source magnets are required, and control magnet (M_C) plays a vital role in determining the functionality. The spin currents from different channels (inputs) of the circuit are believed to be superimposed to generate a resultant spin-polarized current according to majority logic. During magnetization switching of the output nanomagnet, the resultant spin-polarized current from the multiple nanomagnet sources needs to exceed the minimum threshold switching current. The magnetization state of the detector represents the binary output. Magnetization into the plane of the paper is

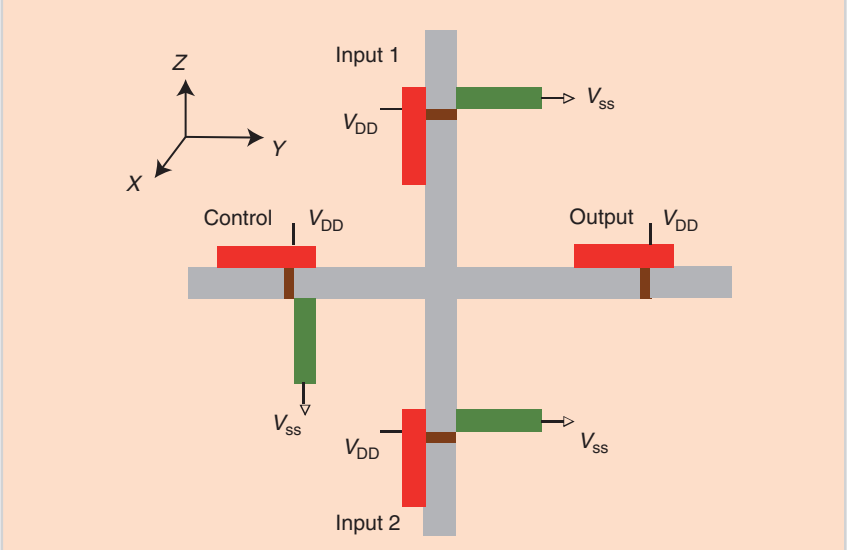


FIGURE 14 The realization of universal gates using ASLD [49].

STT-based devices, circuits, and memory have evolved considerably in recent years.

TABLE 5 A truth table showing the realization of universal ASL gates.

CONTROL	INPUT 1	INPUT 2	OUTPUT			
			POSITIVE V_{DD}		NEGATIVE V_{DD}	
0	0	0	1		0	
0	0	1	1		0	
0	1	0	1	*NAND*	0	*AND*
0	1	1	0		1	
1	0	0	1		0	
1	0	1	0		1	
1	1	0	0	*NOR*	1	*OR*
1	1	1	0		1	

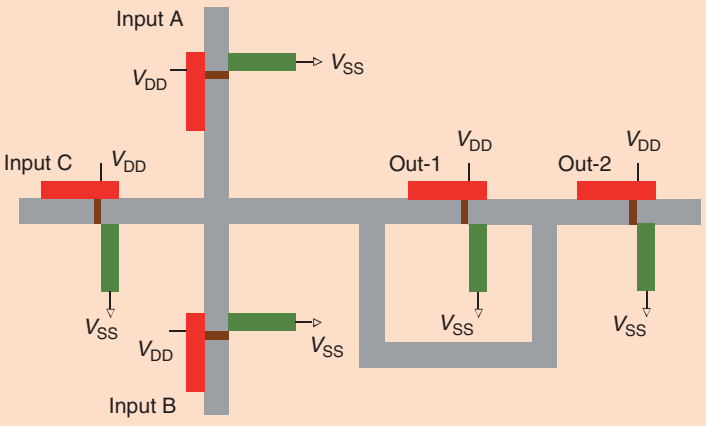


FIGURE 15 The realization of ASL XOR and XNOR logic gates [49].

TABLE 6 A truth table showing the realization of ASL XOR and XNOR.

INPUT A	INPUT B	INPUT C	OUT-1	OUT-2	
0	0	0	1	1	
0	0	1	1	0	
0	1	0	1	0	*XNOR*
0	1	1	0	1	
1	0	0	1	0	
1	0	1	0	1	
1	1	0	0	1	*XOR*
1	1	1	0	0	

considered to be directed toward the $-ve$ x axis and a logic 0, whereas the magnetization out of the plane of the paper is considered as along the $+ve$ x axis and a logic 1.

Table 5 shows the operation of the NAND (NOR). Consider a test input 11, that is, both nanomagnets are in the $+ve$ x direction. For realizing a NAND gate, the magnetization (M_C) of the control is aligned in a direction opposite to the input magnets, that is, along the $-ve$ x axis. The output will invert the majority input signal if the current reaches its switching threshold value and gets aligned in the $-ve$ x direction, giving an output of zero. By reversing the direction of M_C, the same architecture functions as a NOR gate. Furthermore, if a negative supply is used, the same design used for NAND and NOR gates will work as AND and OR gates, respectively.

The realization of a full adder, XOR and XNOR operation is carried out using architecture shown in Figure 15 with a positive V_{DD}. Input A decides XOR or XNOR operation at the out-2 terminal (see Table 6). Moreover, the same architecture is used to implement a full adder circuit, wherein the out-2 terminal is the complement (inverted) of the 3-bit sum operation performed on inputs A, B, and C, and the out-1 terminal implements the complement (inverted) of carry obtained after 3-bit addition of inputs A, B, and C.

The latch is a level-sensitive device. It has two operating modes, a transparent mode when the clock is high and a hold mode when the clock is low. In transparent mode, the input logic state is sampled to the output, whereas in hold mode, the output logic state is maintained at its previous value. The ASL latch is implemented by sandwiching a clocked ASLD between the static input and output ASLDs [49], as shown in Figure 16. For a positive-level triggered latch, when the clock goes high ($V_{CLK} = V_{DD}$), the information from the input is sampled and is transferred to the output. When the clock goes low ($V_{CLK} = 0$),no current can flow toward the output, and it will remain in its previous state. In other words, the data

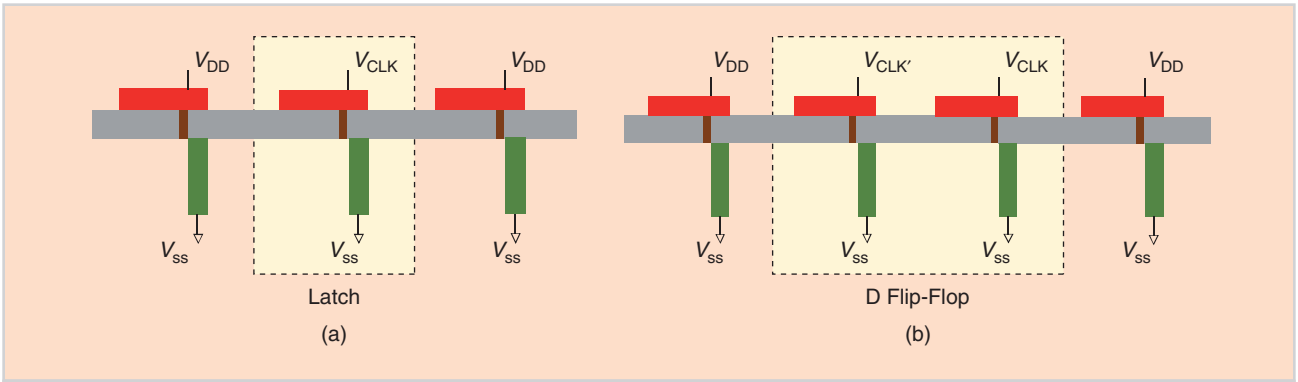


FIGURE 16 The implementation of (a) ASL latch and (b) ASL D flip-flop.

is sampled but not transmitted to the detector when the clock is zero. When the clock becomes high, the path from clock to output is turned on and the data is transmitted to the detector. In a similar manner, D flip-flop is realized designed by cascading two latches, as shown in Figure 16(b).

CONCLUSIONS

STT-based devices, circuits, and memory have evolved considerably in recent years. The progress of nonvolatile memory has already transformed to commercial applications. The recent experimental results of PMA MTJs suggest that reverse connected STT MRAM cells of size as small as $9F^2$ ($F = 65$ nm) can be developed. These PMA MTJs also demonstrate high thermal stability, subnanosecond switching, and scalability.

In the future, STT MRAMs can achieve the performance required for cache memory application while providing the added nonvolatility feature. The challenge is to match device scaling with that of the CMOS technology. At feature size below 40 nm, the high resistance of MTJs is detrimental from the perspective of array density. PMA MTJs need to attain low switching current, high TMR, and high stability without the cost of a large resistance. The novel structured GSHE-based MTJs can be used to overcome problems associated with conventional MTJs by enhancing the efficiency and array density.

The experimental results support the argument behind GSHE MTJs, as the strength of STT generated by GSHE can be three to four times larger. The next step for memory designers is to develop GSHE-based multilevel cell (MLC) memory cells experimentally. The MLCs offer higher array density and less sense circuitry overhead per bit.

The near future is bright while coexisting with the CMOS technology; however, it is important to look further, as the conventional CMOS technology is reaching its scaling limits. Keeping this in mind, both memory and logic designers are working to achieve possible replacements. The VCMA MTJs and ASLDs are two possible successors for memories and logic circuits, respectively. While voltage-controlled switching in VCMA MTJs has been demonstrated experimentally, it has been aided by an external magnetic field. The phenomenon shows too much variability to be viable for producing an alike batch of devices.

ASL suffers from similar challenges, wherein experimental demonstration of STT switching by spin diffusion current is aided by an external magnetic field. Moreover, the device size is quite large. Although the path may be long, spintronics is the way to go to achieve the next switch that inherits all desirable properties of CMOS with added qualities like zero standby power and nonvolatility.

ABOUT THE AUTHORS

Shivam Verma (shivamvermaid@gmail.com) received his M.Tech. degree in microelectronics from the Indian Institute of Technology, Varanasi, in 2012 and his Ph.D. degree in spintronics from the Indian Institute of Technology, Roorkee, in 2016. His research interests include spin-transfer torque-based devices and all-spin logic. He is a Student Member of the IEEE.

Anant Aravind Kulkarni (anantkulkarni2002@gmail.com) received his B.E. degree in electronics engineering from the Shri Guru Gobind Singhji Institute of Engineering and Technology, Nanded, India, in 2002; his first M.Tech. degree in electrical engineering from Uttar Pradesh Technical University, Lucknow, India, in 2009; and his second M.Tech. degree in microelectronics and very-large-scale integration design from the Technocrats Institute of Technology, Bhopal, India, in 2013. He is currently pursuing a Ph.D. degree at the Indian Institute of Technology, Roorkee. His research interests include spintronics-based devices, circuits, and computing. He is a Student Member of the IEEE.

Brajesh Kumar Kaushik (bkk23fec@iitr.ac.in) received his B.E. degree in electronics and communication engineering from the Deenbandhu Chhotu Ram University of Science and Technology, Murthal, India, in 1994; his M.Tech. degree in engineering systems from the Dayalbagh Educational Institute, Agra, India, in 1997; and his Ph.D. degree from the Indian Institute of Technology (IIT), Roorkee, in 2007. He is an associate professor with the Department of Electronics and Communication Engineering, IIT. His research interests include high-speed interconnects, low-power, very-large-scale integration design, nanoscale devices, carbon-nanotube-based designs, organic thin-film transistor design and modeling, and spintronics-based devices and circuits. He is a Senior Member of the IEEE.

REFERENCES

[1] B. Behin-Acin, D. Datta, S. Salahuddin, and S. Datta, "Proposal for an all-spin logic device with built-in memory," *Nature Nanotechnol.*, vol. 5, no. 4, pp. 266–270, Apr. 2010.

[2] G. Binasch, P. Grünberg, F. Saurenbach, and W. Zinn, "Enhanced magnetoresistance in layered magnetic structures with antiferromagnetic interlayer exchange," *Phys. Rev. B*, vol. 39, no. 7, pp. 4828–4830, 1989.

[3] M. N. Baibich, J. M. Broto, A. Fert, F. N. Van Dau, F. Petro, P. Etienne, G. Creuzet, A. Friederich, and J. Chazelas, "Giant magnetoresistance of (001) Fe(001)/(001)Cr magnetic superlattices," *Phys. Rev. Lett.*, vol. 61, no. 21, pp. 2472–2475, 1988.

[4] S. S. P. Parkin, "Dramatic enhancement of interlayer exchange coupling and giant magnetoresistance in Ni81Fe19/Cu multilayers by addition of thin Co interface layers," *Appl. Phys. Lett.*, vol. 61, no. 11, pp. 1358–1360, 1992.

[5] D. D. Tang and Y. J. Lee, *Magnetic Memory Fundamentals and Technology.* Cambridge, U.K.: Cambridge Univ. Press, 2010, ch. 3–6.

[6] J. C. Slonczewski, "Current-driven excitation of magnetic multilayers," *J. Magn. Magn. Mater.*, vol. 159, no. 1–2, pp. L1–L7, 1996.

[7] H. J. G. Draaisma and W. J. M. de Jonge, "Surface and volume anisotropy from dipole–dipole interactions in ultrathin ferromagnetic films," *J. Appl. Phys.*, vol. 64, no. 7, p. 3610, 1988.

[8] M. T. Johnson, P. J. H. Bloemen, F. J. A. Den Broeder, and J. J. De Vries, "Magnetic anisotropy in metallic multilayers," *Rep. Prog. Phys.*, vol. 59, no. 11, pp. 1409–1458, 1996.

[9] M. Tsoi, A. G. M. Jansen, J. Bass, W.-C. Chiang, M. Seck, V. Tsoi, and P. Wyder, "Excitation of a magnetic multilayer by an electric current," *Phys. Rev. Lett.*, vol. 80, no. 19, pp. 4281–4284, 1998.

[10] J. Z. Sun, "Current-driven magnetic switching in manganite trilayer junctions," *J. Magn. Magn. Mater.*, vol. 202, no. 1, pp. 157–162, 1999.

[11] E. B. Myers, "Current-induced switching of domains in magnetic multilayer devices," *Science*, vol. 285, no. 5429, pp. 867–870, 1999.

[12] M. D. Stiles and J. Miltat, "Spin-transfer torque and dynamics," *Top. Appl. Phys.*, vol. 101, pp. 225–308, 2006.

[13] A. A. Timopheev, R. Sousa, and M. Chshiev, "Respective influence of in-plane and out-of-plane spin-transfer torques in magnetization switching of perpendicular magnetic tunnel junctions," *Phys. Rev. B*, vol. 92, no. 10, pp. 104430, Sept. 2015.

[14] A. Brataas, A. D. Kent, and H. Ohno, "Current-induced torques in magnetic materials," *Nat. Mater.*, vol. 11, no. 5, pp. 372–381, 2012.

[15] R. K. Tiwari, M. H. Jhon, N. Ng, D. J. Srolovitz, and C. K. Gan, "Current-induced switching of magnetic tunnel junctions: Effects of field-like spin-transfer torque, pinned-layer magnetization orientation, and temperature," *Appl. Phys. Lett.*, vol. 104, no. 2, pp. 022413, 2014.

[16] S. Ikeda, H. Sato, M. Yamanouchi, H. Gan, K. Miura, K. Mizunuma, S. Kanai, S. Fukami, F. Matsukura, N. Kasai, and H. Ohno, "Recent progress of perpendicular anisotropy magnetic tunnel junctions for nonvolatile VLSI," *Spin*, vol. 2, no. 3, p. 1240003, Sept. 2012.

[17] S. Ikeda, J. Hayakawa, Y. Ashizawa, Y. M. Lee, K. Miura, H. Hasegawa, M. Tsunoda, F. Matsukura, and H. Ohno, "Tunnel magnetoresistance of 604% at 300K by suppression of Ta diffusion in CoFeB/MgO/CoFeB pseudo-spin-valves annealed at high temperature," *Appl. Phys. Lett.*, vol. 93, no. 8, p. 082508, Aug. 2008.

[18] R. Sbiaa, R. Law, E. L. Tan, and T. Liew, "Spin transfer switching enhancement in perpendicular anisotropy magnetic tunnel junctions with a canted in-plane spin polarizer," *J. Appl. Phys.*, vol. 105, no. 1, p. 013910, 2009.

[19] C.-Y. You, "Reduced spin transfer torque switching current density with non-collinear polarizer layer magnetization in magnetic multilayer systems," *Appl. Phys. Lett.*, vol. 100, no. 25, p. 252413, June 2012.

[20] H. Liu, D. Bedau, D. Backes, J. A. Katine, J. Langer, and A. D. Kent, "Ultrafast switching in magnetic tunnel junction based orthogonal spin transfer devices," *Appl. Phys. Lett.*, vol. 97, no. 24, pp. 16–19, 2010.

[21] N. Nagaosa, J. Sinova, S. Onoda, A. H. MacDonald, and N. P. Ong, "Anomalous Hall effect," *Rev. Mod. Phys.*, vol. 82, no. 2, pp. 1539–1592, May 2010.

[22] J. E. Hirsch, "Spin Hall effect," *Phys. Rev. Lett.*, vol. 83, no. 9, pp. 1834–1837, Aug. 1999.

[23] A. Hoffmann, "Spin Hall effects in metals," *IEEE Trans. Magn.*, vol. 49, no. 10, pp. 5172–5193, 2013.

[24] L. Liu, C.-F. Pai, Y. Li, H. W. Tseng, D. C. Ralph, and R. A. Buhrman, "Spin-torque switching with the giant spin Hall effect of tantalum," *Science*, vol. 336, no. 6081, pp. 555–558, 2012.

[25] T. Tanaka, H. Kontani, M. Naito, T. Naito, D. S. Hirashima, K. Yamada, and J. Inoue, "Intrinsic spin Hall effect and orbital Hall effect in 4*d* and 5*d* transition metals," *Phys. Rev. B*, vol. 77, no. 16, p. 165117, 2008.

[26] M. Yamanouchi, L. Chen, J. Kim, M. Hayashi, H. Sato, S. Fukami, S. Ikeda, F. Matsukura, and H. Ohno, "Three terminal magnetic tunnel junction utilizing the spin Hall effect of iridium-doped copper," *Appl. Phys. Lett.*, vol. 102, no. 21, p. 212408, 2013.

[27] Q. Hao and G. Xiao, "Giant spin Hall effect and switching induced by spin-transfer torque in a W/Co40Fe40B20/MgO structure with perpendicular magnetic anisotropy," *Phys. Rev. Applied*, vol. 3, no. 3, p. 034009, 2015.

[28] M. Jamali, J. S. Lee, J. S. Jeong, F. Mahfouzi, Y. Lv, Z. Zhao, B. Nikolic, K. A. Mkhoyan, N. Samarth, and J.-P. Wang, "Giant spin pumping and inverse spin Hall effect in the presence of surface spin-orbit coupling of topological insulator Bi2Se3," *Nano Lett.*, vol. 15, no. 10, pp. 7126–7132, Sept. 2015.

[29] W.-G. Wang, M. Li, S. Hageman, and C. L. Chien, "Electric-field-assisted switching in magnetic tunnel junctions," *Nat. Mater.*, vol. 11, no. 1, pp. 64–68, 2011.

[30] F. Matsukura, Y. Tokura, and H. Ohno, "Control of magnetism by electric fields," *Nature Nanotechnol.*, vol. 10, no. 3, pp. 209–220, 2015.

[31] P. K. Amiri and K. L. Wang, "Voltage-controlled magnetic anisotropy in spintronic devices," *Spin*, vol. 2, no. 3, p. 1240002, 2012.

[32] N. A. Pertsev, "Origin of easy magnetization switching in magnetic tunnel junctions with voltage-controlled interfacial anisotropy," *Sci. Rep.*, vol. 3, p. 2757, Sept. 2013.

[33] S. Kanai, Y. Nakatani, M. Yamanouchi, S. Ikeda, H. Sato, F. Matsukura, and H. Ohno, "Magnetization switching in a CoFeB/MgO magnetic tunnel junction by combining spin-transfer torque and electric field-effect," *Appl. Phys. Lett.*, vol. 104, no. 21, p. 212406, 2014.

[34] S. Srinivasan, A. Sarkar, B. Behin-Aein, and S. Datta, "All-spin logic device with inbuilt nonreciprocity," *IEEE Trans. Magn.*, vol. 47, no. 10, pp. 4026–4032, Oct. 2011.

[35] C.-C. Lin, A. V. Penumatcha, Y. Gao, V. Q. Diep, J. Appenzeller, and Z. Chen, "Spin transfer torque in a graphene lateral spin valve assisted by an external magnetic field," *Nano Lett.*, vol. 13, no. 11, pp. 5177–5181, Nov. 2013.

[36] C. J. Lin, S. H. Kang, Y. J. Wang, K. Lee, X. Zhu, W. C. Chen, X. Li, W. N. Hsu, Y. C. Kao, M. T. Liu, W. C. Chen, Y. Lin, M. Nowak, N. Yu, and L. Tran, "45nm low power CMOS logic compatible embedded STT MRAM utilizing a reverse-connection 1T/1MTJ cell," in *Proc. 2009 IEEE Int. Electron Devices Meet. (IEDM)*, pp. 279–282.

[37] P. C. Read, T. Kawahara, R. Takemura, K. Miura, J. Hayakawa, S. Ikeda, Y. M. Lee, R. Sasaki, Y. Goto, K. Ito, T. Meguro, F. Matsukura, H. Takahashi, H. Matsuoka, H. Ohno, A. A. V Mb, and S. Ram, "2 Mb SPRAM (spin-transfer torque RAM) with bit-by-bit bi-directional current write," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 109–120, 2008.

[38] Z. Li and S. Zhang, "Thermally assisted magnetization reversal in the presence of a spin-transfer torque," *Phys. Rev. B*, vol. 69, no. 13, p. 134416, Apr. 2004.

[39] T. Kawahara, K. Ito, R. Takemura, and H. Ohno, "Spin-transfer torque RAM technology: Review and prospect," *Microelectron. Reliab.*, vol. 52, no. 4, pp. 613–627, Apr. 2012.

[40] S. Ikeda, K. Miura, H. Yamamoto, K. Mizunuma, H. D. Gan, M. Endo, S. Kanai, J. Hayakawa, F. Matsukura, and H. Ohno, "A perpendicular-anisotropy CoFeB-MgO magnetic tunnel junction," *Nat. Mater.*, vol. 9, no. 9, pp. 721–724, Sept. 2010.

[41] G. Jan, Y.-J. Wang, T. Moriyama, Y.-J. Lee, M. Lin, T. Zhong, R.-Y. Tong, T. Torng, and P.-K Wang, "High spin torque efficiency of magnetic tunnel junctions with MgO/CoFeB/MgO free layer," *Appl. Phys. Express,* vol. 5, no. 9, pp. 093008, 2012.

[42] L. Thomas, G. Jan, J. Zhu, H. Liu, Y.-J. Lee, S. Le, R.-Y. Tong, K. Pi, Y.-J. Wang, D. Shen, R. He, J. Haq, J. Teng, V. Lam, K. Huang, T. Zhong, T. Torng, and P.-K. Wang, "Perpendicular spin transfer torque magnetic random access memories with high spin torque efficiency and thermal stability for embedded applications (invited)," *J. Appl. Phys.*, vol. 115, no. 17, p. 172615, May 2014.

[43] A. Lyle, J. Harms, S. Patil, X. Yao, D. J. Lilja, and J.-P. Wang, "Direct communication between magnetic tunnel junctions for nonvolatile logic fan-out architecture," *Appl. Phys. Lett.*, vol. 97, no. 15, p. 152504, Oct. 2010.

[44] H. Mahmoudi, T. Windbacher, V. Sverdlov, and S. Selberherr, "Reliability analysis and comparison of implication and reprogrammable logic gates in magnetic tunnel junction logic circuits," *IEEE Trans. Magn.*, vol. 49, no. 12, pp. 5620–5628, Dec. 2013.

[45] Y. Seo, X. Fong, K. Kwon, and K. Roy, "Spin-Hall magnetic random-access memory with dual read/write ports for on-chip caches," *IEEE Magn. Lett.*, vol. 6, p. 300204, Apr. 2015.

[46] Y. Kim, S. H. Choday, and K. Roy, "DSH-MRAM: Differential spin Hall MRAM for on-chip memories," *IEEE Electron Device Lett.*, vol. 34, no. 10, pp. 1259–1261, 2013.

[47] W. Kang, W. Zhao, Z. Wang, and Y. Zhang, "DFSTT-MRAM: Dual functional STT-MRAM cell structure for reliability enhancement and 3D MLC functionality," *IEEE Trans. Magn.*, vol. 50, no. 6, p. 3400207, 2014.

[48] Y. Kim, X. Fong, K. Kwon, M. Chen, and K. Roy, "Multilevel spin-orbit torque MRAMs," *IEEE Trans. Magn.*, vol. 62, no. 2, pp. 561–568, 2015.

[49] V. Calayir, D. E. Nikonov, S. Manipatruni, and I. A. Young, "Static and clocked spintronic circuit design and simulation with performance analysis relative to CMOS," *IEEE Trans. Circuits Syst. I. Reg. Papers*, vol. 61, no. 2, pp. 393–406, Feb. 2014.

[50] A. Sarkar, S. Srinivasan, and S. Datta, "Modeling all spin logic: Multi-magnet networks interacting via spin currents," in *Proc. 2011 IEEE Int. Electron Devices Meeting (IEDM)*, pp. 247–250.

N