Low Power Management Unit with Load Regulation using DC-DC Switched Capacitor Converters in 0.18μm CMOS

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***Abstract*—A power management unit (PMU) with battery extender and output load regulation is presented using 0.18μm CMOS technology. For designing few sub-circuits of the PMU, subthreshold region of MOSFET is utilized, which significantly contributes to achieve low power operation. The proposed PMU consists of a voltage regulator, a voltage monitor, a battery backup module and two DC-DC Switched Capacitor (SC) Converters. The regulator output voltage V_{OUT} is regulated at 0.95 V and 0.968 V at input voltages of 0.98 V and 1.33 V respectively. To ensure continuous operation at the load circuit, a battery extender module is implemented in case of unavailability of EH source. The power consumption of the PMU at input voltages of 0.98 V and 1.33 V is 46nW and 1.567 μW respectively. Near threshold operation is ensured at the load side by further regulating the voltage at the output to 0.67 V and 0.5 V using 3:2 and 2:1 SC Converters respectively. The current consumption of the 3:2 and 2:1 SC Converters is 748 nA and 751 nA respectively. The proposed PMU can deliver output current up to 1 mA at 1.33 V of input voltage and is suitable for numerous applications where low power operation is essential as it consumes a small amount of power.**

***Keywords*—PMU, 0.18 μm CMOS, Switched Capacitor**

I. Introduction

Energy harvesting helps in operating electronics in the absence of a conventional power source and remove the cumbersome task of battery substitution. There are different energy harvesting sources available which convert ambient energy into useful electrical power [1], [2] such as solar, thermal, vibrational, RF and other methods. Among them solar energy harvesting is widely used to deliver appropriate power output for low voltage, low power applications.

To meet the energy budget of emerging ultra low power (ULP) applications, several tiny solar cells can be stacked together but they need some low dropout (LDO) regulation circuitry as the electronics cannot be driven directly. To get a constant supply from the harvesters with the help of regulator circuits in PMUs [2–4], it is essential to manage the power properly.

In order to design power efficient PMUs, several efforts have been made [3–5]. The output voltage of solar DC harvesters lie in the range 0.27 V to 0.45 V. In addition to LDOs (used to regulate the output voltage), charge pump [2], [4] circuits are used to further regulate this voltage to below 1 V range. In the absence of EH source, battery backup modules are implemented [6] to obtain continuous operation at the load side.

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The output voltage at the load side can be further regulated using DC-DC regulators [7] in order to obtain low power operation. Various DC–DC regulator categories are available for this purpose. However the most popular among them are linear and switching regulators. Authors in [8] establish that switching regulators (converters) have better performance in terms of efficiency as compared to linear converters. Switching converters are further divided into: Inductor based switching converters and Capacitor-based converters. Switched capacitor converters [9] are more preferable than inductor-based converters due to easier on-chip integration as compared to inductors.

In this work, we present an ULP PMU circuit which achieves lowest power consumption attributed to subthreshold and standard CMOS circuits. The structure of the paper is as follows: Section II describes the architecture of the PMU. Section III discusses the design considerations of the PMU. Different PMU sub-blocks and simulation results of the PMU are explained in Section IV. Followed by conclusion in Section V.

II. Proposed Architecture

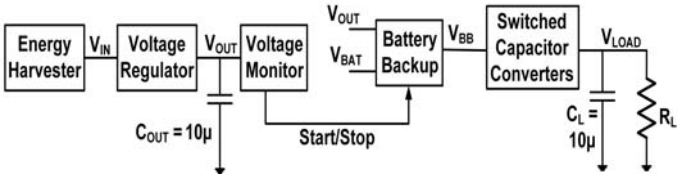

Fig. 1: Block Diagram of the Proposed Work

The proposed PMU is composed of an energy harvester, a voltage regulator, a voltage monitor, a battery backup module and switched capacitor converters along with resistors and capacitors, as can be seen from Fig. 1. The energy provided by solar energy harvester acts as a primary input source for the PMU. This input voltage V_{IN} is regulated by the voltage regulator to get a continual output voltage (V_{OUT}).

The circuit diagram of the PMU is depicted in Fig. 2. The voltage monitor ensures that enough output voltage (V_{OUT}), is available for the load. The voltage monitor disconnects the node V_{BB} from the regulator output when V_{OUT} comes under an acceptable pre-defined lower threshold voltage ($0.6V_{OUT}$ in our case).

When an EH source does not provide sufficient voltage to the load circuit, an external battery is used to replace it. The Start/Stop signal from the voltage monitor as shown in Fig. 2 which is used to decide the availability of the regulator voltage or battery voltage at the V_{BB} node. In this manner, the availability of uninterrupted output voltage is ensured.

In the last stage of the PMU, two SC DC-DC Converters are implemented which regulate the load voltage (V_{LOAD}) between 0.67 V and 0.5 V. We observe that by doing so, the PMU circuit offers an added advantage of load circuits being powered at near threshold voltages.

The proposed PMU is designed with the assumption that when EH source is available and PMU starts working with a cold start. In this work, two series connected solar cells are used to provide input to the PMU (see Fig. 2). The solar cells equivalent model [10] is characterized by 1 mA of short circuit current I_{SC} and 1.76 V of the open circuit voltage as shown in Fig. 3. The maximum power extracted from the solar cells is 1.29 mW.

III. Design Considerations

The subthreshold region is preferred to obtain low power operation. The voltage regulator and voltage monitor blocks are designed in the subthreshold region of MOSFET (without the pass element used in the voltage regulator). To design the sub-circuits the following conditions are mandatory: $|V_{TH}| > |V_{GS}|$ and $|V_{DS}| \geq 100$mV.

For the subthreshold region, drain current [11] for NMOS and PMOS is estimated by following equation:

$$I_D = I_0 \frac{W}{L} \left(e^{\frac{|V_{GS}|-|V_{TH}|}{nV_T}} \right) \left(1 - e^{\frac{-|V_{DS}|}{V_T}} \right) \quad (1)$$

Since $\left(1 - e^{\frac{-|V_{DS}|}{V_T}} \right) \equiv 1$, eqn. (1) results in,

$$I_D = I_0 \frac{W}{L} \left(e^{\frac{|V_{GS}|-|V_{TH}|}{nV_T}} \right) \quad (2)$$

where, I_0 off current is given by following equation:

$$I_0 = 2 \times \mu C_{ox} \times n \times {V_T}^2 \quad (3)$$

where, subthreshold slope parameter n lies between 1 to 2 [11], μ represents the mobility of electrons (or holes) and C_{ox} denotes the gate oxide capacitance. $|V_{GS}|$ is gate to source and $|V_{DS}|$ is drain to source voltage. $\frac{W}{L}$ indicates aspect ratio of MOS transistor. $|V_{TH}|$ is the threshold voltage of MOSFET and V_T shows the thermal equivalent voltage of temperature.

For the subthreshold region of MOSFET, the output resistance and the transconductance are given as:

$$R_{out} = \frac{nV_T}{\lambda I_D}; \quad g_m = \frac{I_D}{nV_T} \quad (4)$$

where, λ denotes the channel length modulation parameter.

The gain of the error amplifier shown in Fig. 2, is calculated by: A_V;

$$A_V = R_{out} \times g_{meq} \quad (5)$$

where, R_{out} shows the equivalent output resistance and g_{meq} represents transconductance of the error amplifier,

Frequency of a SC circuit is given by,

$$f = \frac{1}{R \times C} \quad (6)$$

where, R = resistance and C = capacitance of a SC circuit.

Resistance of a transmission gate is given by,

$$R = (Rn||Rp) \quad (7)$$

where Rn and Rp are the resistances of NMOS and PMOS switches of a transmission gate respectively.

Rn and Rp are given by,

$$Rn(Rp) = \frac{1}{\mu C_{ox} \times \frac{W}{L} \times (|V_{GS}| - |V_{TH}|)} \quad (8)$$

The designed SC Converters have a switching frequency of 13.4 kHz which is obtained by choosing the value of capacitance and resistance as 10 pF and 7.46 MΩ respectively.

Efficiency (η) of a PMU is given by:

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100\% = \frac{I_{OUT} \times V_{OUT}}{V_{IN} \times I_{IN}} \times 100\% \quad (9)$$

where P_{OUT}, V_{OUT}, I_{OUT}, P_{IN}, V_{IN} and I_{IN} are output power, output voltage, output current, input power, input voltage and input current of the PMU respectively.

TABLE I: Model Parameters

Parameter	PMOS	NMOS
Threshold Voltage of MOSFET, $V_{th}(V)$	-0.518	0.4616
Technology Parameter, $k = \mu C_{ox}(mA/V^2)$	0.0625	0.316
Subthreshold Slope Factor, n	1.6	1.4
Channel Length Modulation Parameter, $\lambda(V^{-1})$	-0.95	0.92

Model parameters given in Table I are used for the sizing of transistors used in various circuits of the PMU. The design considerations begin with the bias currents and bias voltages for the sub-blocks of the PMU. The proportional to absolute temperature (PTAT) current reference of 1 nA is designed using eqns. (2) and (3), which is the basic sub-circuit for the regulator. The reference voltage, voltage divider circuit and bias voltages for error amplifier are designed using this current reference. Sizing of the various transistors of the error amplifier is calculated by previously designed bias currents, bias voltages and the gain parameter (using eqns. (4) and (5)). The error amplifier is used as a comparator for the voltage monitor as well.

Battery extender module is designed by implementing switching logic between the external battery and the EH source. At last, SC Converters are designed using eqn. (6). Resistors are implemented using MOS switches (transmission gates) to use optimal area and are given by eqns. (7) and (8).

IV. Sub-blocks of PMU

A. Voltage Regulator

Basic building blocks of voltage regulator are a pass element, a voltage divider, a reference voltage, an error amplifier and an output capacitance (C_{OUT}) as shown in Fig. 2. The voltage divider network has to be adjusted continuously to which the variable resistance is provided by R1 and R2 to

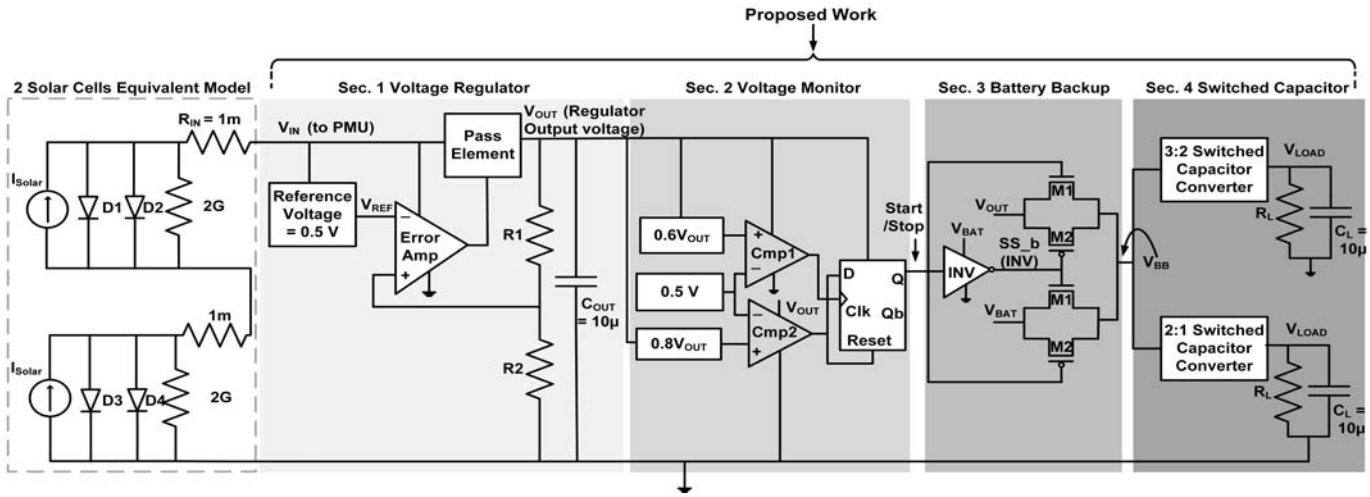

Fig. 2: Circuit Diagram of the Proposed Work

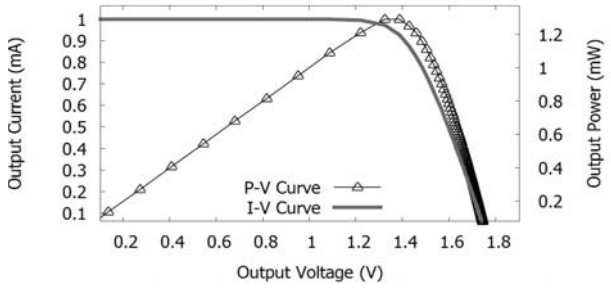

Fig. 3: Characteristics of Solar Cells

sustain a constant voltage at the regulator output (V_{OUT}). The regulator output voltage (V_{OUT}) is expressed as:

$$V_{OUT} = V_{REF}\left[1 + \left(\frac{R1}{R2}\right)\right] \tag{10}$$

Current flowing through the pass element gets controlled by the error amplifier in order to regulate the V_{OUT}. In the frequency response of an amplifier, a 46.39 dB gain and unity gain bandwidth (UGBW) at 206 kHz is observed.

B. Voltage Monitor

The voltage monitor [3] comprises of two comparators and an active low reset DFF (D flip-flop) as shown in Fig. 2. The voltage monitor generates a Start/Stop signal for enabling or disabling the regulator output voltage at the load side. The Start signal is generated at 0.76 V(= 0.8×0.95 V) whereas Stop is generated at 0.57 V(= 0.6×0.95 V). Voltages $0.6V_{OUT}$ and $0.8V_{OUT}$ are chosen as lower and upper threshold voltages for the voltage monitor respectively. These values can be different for other applications. When V_{OUT} meets the upper threshold voltage (0.8 V), voltage monitor ensures that the V_{BB} node is connected to V_{OUT} via the upper transmission gate in the battery backup module. It connects V_{BB} node to V_{BAT} as soon as V_{OUT} drops below the lower threshold voltage (0.6 V).

C. Battery Extender

A battery backup module is implemented to energize the load circuit when EH source is either unavailable or insufficient to provide the required energy to the load circuit. The value of external battery voltage is chosen as 1 V as regulator regulates the V_{OUT} at 0.95 V and 0.968 V and it can be selected a different value as per the system requirements.

There is a need for control signal which selects either the regulator voltage or the battery voltage to be reached at the V_{BB} node. Start/Stop signal from the voltage monitor is used as a control signal. This block ensures the uninterrupted operation at the load side regardless of the availability of the EH source. The power consumption of this module is 10 nW.

The functionality of the battery backup module is as follows. The upper transmission gate in Fig. 2 connects the regulator output V_{OUT} to the V_{BB} as soon as the V_{OUT} reaches to $0.8V_{OUT}$. The battery voltage is available at the V_{BB} node when the V_{OUT} drops below $0.6V_{OUT}$.

D. DC-DC Switched Capacitor Converters

A switched capacitor circuit consists of switches and capacitors to control and distribute charge [9]. It is used as a power converter to generate multiple voltages from a single power supply to power various components of integrated circuits (ICs). Two DC-DC SC Converters namely 3:2 and 2:1 converters are implemented to regulate the PMU voltage at 0.67 V and 0.5 V respectively. A RC ring oscillator is used to supply clock for the SC circuit. A PTAT current reference is used to control the current of the RC oscillator which reduces the power consumption of the same.

1) Switched Capacitor 3:2 Converter: Fig. 4 shows a circuit diagram of a 3:2 SC Converter, which consists of S1 to S7 switches, and 4 capacitors C_1, C_2, Co and C_{filter}. Filtering capacitor, C_{filter} is used to remove fluctuations at the converter output. V_{BB} is the input and V_{LOAD} is the output voltage of the converter.

The working of 3:2 SC Converter [9] is now described: When clk signal goes high and clk_b signal representing the complementary clock, becomes low (Phase 1); switches S1, S3, S5, and S6 are turned on making $C_1||C_2$ in series with Co and gives an output voltage equivalent to two by three times of the input voltage (if $C_1 = C_2 = Co$). In phase 2, the clk signal becomes low (clk_b signal at logic high level)

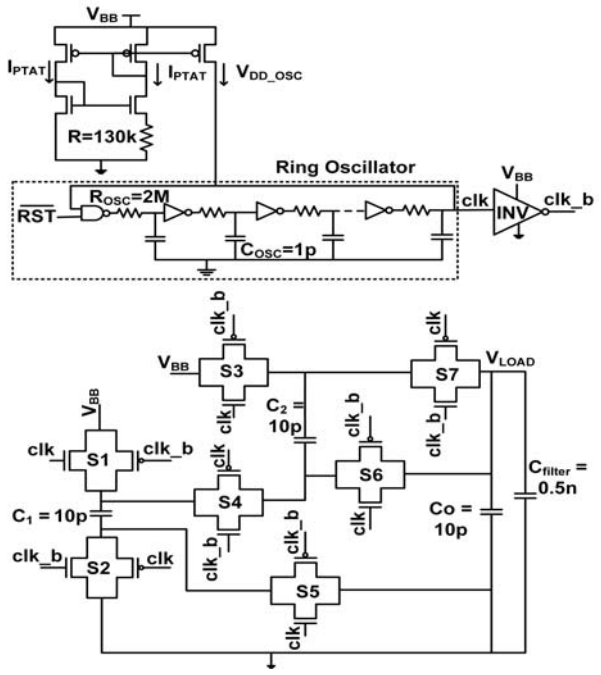

Fig. 4: Circuit Diagram of 3:2 Switched Capacitor Converter

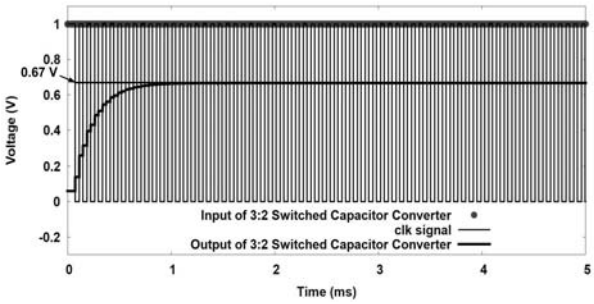

Fig. 5: Transient Response of 3:2 Switched Capacitor Converter

switches S2, S4, and S7 are turned on and making a series combination of C_1 and C_2 in parallel with Co which in turns provides an output voltage of two by three times than its input voltage (if $C_1 = C_2 = Co$).

Ring oscillator provides a switching frequency of 125 kHz to these SC Converters. Fig. 5 shows the transient response of 3:2 voltage converter, which assures that the output voltage is down converted from 1 V (V_{BB}) to 0.67 V (V_{LOAD}), which is two by three times of input voltage ($\sim$ 1 V in our case). The 3:2 SC Converter consumes 748 nW of power.

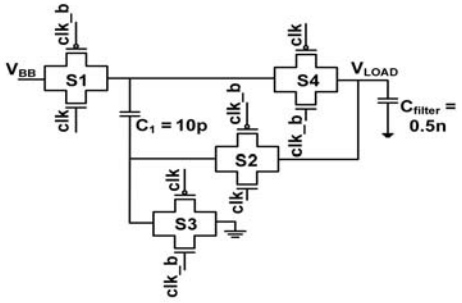

Fig. 6: Circuit Diagram of 2:1 Switched Capacitor Converter

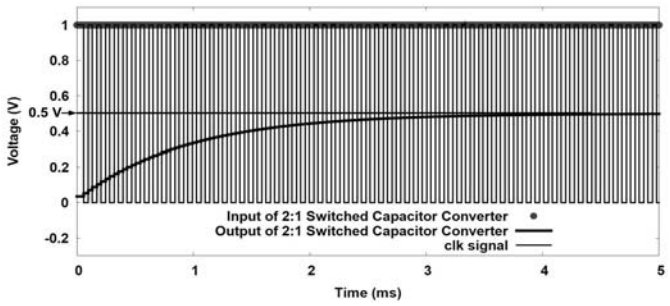

Fig. 7: Transient Response of 2:1 Switched Capacitor Converter

2) Switched Capacitor 2:1 Converter: A 2:1 SC Converter, shown in Fig. 6, consists of S1 to S4 switches and 2 capacitors C_1 and C_{filter}. Working principle of 2:1 SC Converter is described in two parts according to the clk signal; Phase 1: When clk is at logic high (clk_b signal is at logic low level) and Phase 2: When the clk signal goes to logic low (clk_b goes to logic high). During Phase 1, switches S1 and S2 are on and as a result the capacitor C_1 is placed between the input node V_{BB} and the output node V_{LOAD}. Capacitor C1 is charged up from the charge drawn from the V_{BB} node. In phase 2, switches S3 and S4 are turned on and as a result, C_1 is bridged between V_{LOAD} and ground and thus, previously stored charge on C_1 is shifted to the output. V_{BB} and V_{LOAD} voltages for the converter are 1 V and 0.5 V respectively.

The transient response of 2:1 voltage converter as shown in Fig. 7, ensures that the load voltage is correctly down converted from 1 V (V_{BB}) to 0.5 V (V_{LOAD}), which is half the value of input voltage 1V. The power consumption of the converter is 751 nW.

E. Simulation Results and Discussion

The simulations for the PMU sub-blocks were carried out on the schematic level using 0.18μm CMOS technology model files. For the simulations, the load capacitor value is selected as 10 μF which represents a sufficient capacitance value for most ULP applications. Simulations are carried out for an input current: I_{Solar} $\sim$1 mA, V_{IN} = 1.33 V and V_{OUT} = 0.968 V. The simulation results of different sub-blocks of the PMU are shown in Table II. From the simulations, it is observed that PMU consumes 1.552 μA and the rest is delivered to R_L. On the first pass, the efficiency of PMU is 72.3% (given by eqn. (9)) without the switched capacitor converters.

The proposed PMU is compared with the existing PMUs in terms of power consumption, output current and regulated voltage. We selected I_{Solar} and V_{IN} based on our application. Different values for the same can be selected in accordance with the application. In the mentioned literature [3–5] value of V_{IN} is chosen as 0 to 2.2 V, 270 mV and $\leq V_{TH}(\sim$ 0.4 V), respectively and I_{Solar} values are not provided.

Table II presents the current and power consumption of the individual blocks of the PMU. The results are obtained at two different input voltages at 0.98 V and 1.33 V. The total current consumed by the PMU at 0.98 V and 1.33 V is 42 nA and 54 nA, respectively, with the exception of SC Converters. The 3:2 and 2:1 SC Converters consumes 748 nW and 751 nW at 1 V of an input voltage. The comparison of the designed PMU

TABLE II: Current and Power Consumption of the PMU Sub-blocks

PMU Sub-block	Individual Blocks of PMU Sub-block	Current (A) (@ 0.98 V)	Power (W) (@ 0.98 V)	Current (A) (@ 1.33 V)	Power (W) (@ 1.33 V)
Voltage Regulator	error amplifier	11.8 n	11.2 n	14.7 n	20 n
	Reference Voltage	2.56 n	2.43 n	2.9 n	4 n
	Voltage Divider	0.84 n	0.8 n	0.97 n	1.3 n
	Pass Element	1.5 p	1.43 p	2 p	2.7 p
Voltage Monitor	Two Comparators	21.8 n	20.7 n	22.15 n	29.5 n
	DFF	10.16 p	9.65 p	10.32 p	13.7 p
Battery Extender	-	10 n	10 n	12 n	12 n
@ PMU (without SC Converters)	-	48 n *	46 n	54 n*	68 n
Switched Capacitor Converters	3:2 Converter	-	-	748 n	748 n
	2:1 Converter	-	-	751 n	751 n
Total	-	48 n	46 n	1.552 μ	1.567 μ

* The PMU consumes total 48 nA and 54 nA at 0.98 V and 1.33 V, respectively because insulator resistor consumes 1 nA, which is used to decrease the leakage current through the output capacitor C_{OUT}.

TABLE III: Performance Comparison with Reported Research in Literature

Parameter	This Work		[3]	[4]	[5]	[13]
	@V_{IN} = 0.98 V & @I_{Solar} = 70 nA	@V_{IN} = 1.33 V & @I_{Solar} = 1 mA				
Regulated Voltage (V)	0.95	0.968	1.8	1.4	1.0	NA$^{\phi}$
Power Dissipation (W)	46 n	1.567 μ	655 n	2.62 μ	256 μ	50 n *
Load Current (A)	32 n	1.0 m	25 m	5 μ	0.6-1.1 m	NA$^{\phi}$
Technology (m)	0.18 μ		0.18 μ	0.13 μ	0.18 μ	65 n
Operating Region	Subthreshold		Subthreshold	Strong Inversion	Strong Inversion	Subthreshold

* [13] has 50 nW power consumption for Voltage Monitor Block only.
# Not Reported
$^{\phi}$ Not Applicable

with reported research is presented in Table III. The designed PMU is observed to offer power and performance benefits as compared to the reported works in [4], [5] and [13].

V. Conclusion

The ultra low power PMU, presented in this work provides energy autonomy to circuits, utilizing the advantage of the sub-threshold region of operation of the transistors. The regulator output voltage V_{OUT} occurs at 0.95 V and 0.968 V at 0.98 V and 1.33 V input voltages and consumes 46 nW and 1.567 μW power, respectively. By implementing the battery backup module, continuous power delivery at the load side is ensured. At the last stage of the PMU, two DC-DC SC Converters are employed in 3:2 and 2:1 converters, to further regulate the voltage at 0.67 V and 0.5 V respectively, with an aim to obtain low power operation and consume 748 nW and 751 nW at 1 V of an input voltage, respectively. The availability of 3 different voltages on a single system make PMU a useful candidate for various power conscious applications.

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