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CMOS Power Management Unit Along with Load Regulation Using Switched Capacitor Converters

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In this paper, a power management unit (PMU) with battery backup and output load regulation using switched capacitor converters using 0.18 μm Complimentary Metal Oxide Semiconductor technology is presented. Low power consumption is obtained by employing subthreshold design methods. The main building blocks of the PMU are a voltage regulator, a voltage monitor, a battery backup and switched capacitor (SC) converters. The voltage regulator has an output voltage V_{OUT} at 0.95 V and 0.968 V at input voltages of 0.98 V and 1.33 V, respectively. Perpetual operation at the load side is confirmed by implementing a battery backup module, which provides the battery voltage to the load circuit when the output voltage of the energy harvesting (EH) source is insufficient. The presented PMU consumes 46 nW at 0.98 V and 3.919 μW with SC converters at 1.33 V. Different voltages can be tapped from the PMU from the 3:2, 2:1, 3:1, 4:1 and 5:1 down converters that provide output voltages of 0.67 V, 0.5 V, 0.33 V, 0.25 V and 0.2 V to the load, respectively. The maximum current that can be delivered by the PMU is 1 mA at an input voltage of 1.33 V and is adequate for many low power applications.

Keywords: Power Management Unit, Switched Capacitor, 0.18 μm CMOS, Energy Harvesting.

1. INTRODUCTION

Energy harvesting[1–3] in piezoelectric, RF, solar, thermoelectric and microbial fuel cells transform freely available ambient energy into useful energy.[1–6] Out of them, solar energy harvesting[2,5,7,8] receives maximum attention as it delivers the desired output power for low power applications, and abundant reliable. Several tiny solar cells stacked together can fulfill the energy requirements for low power circuits but the harvested energy is not usable directly. Solar harvesters have an output voltage range of 270 mV to 450 mV, that is further regulated by charge pump[5,8] or equivalent circuits for voltage regulation. Low drop out (LDO) regulations are required in these power management circuits prior to feeding to the load circuits. It is necessary to manage the harvested power properly to obtain a reliable supply for electronic circuits through the use of PMUs.[4,7–9] There have been numerous techniques discussed in literature for such PMU designs.[4,5,7,8] Additionally circuits powered by energy harvesters, battery extender modules[10] are often employed that selects the power supply between an external battery and an EH source to assure an undisturbed operation.

In low voltage, low power applications, the microcontrollers, sensor interfaces, radio circuits are operated at different voltages to obtain power benefits. Therefore, it is beneficial to generate multiple voltages from a single power supply[11] for efficient power management. DC–DC converters[12,13] are best suited for regulation of the output voltage of the PMUs. Several DC–DC converters in switching and linear converters[7] are used widely. As mentioned in reference,[14] switching converters are adopted as they have higher efficiency than the linear converters. Out of the inductor based and capacitor based switching converters, switched capacitor converters[11] are more efficient and adopted because of their easier on-chip integration. In this work, a low power EH PMU is presented which consumes very low power due to circuits that uses a combination of subthreshold and standard CMOS circuits. The paper is structured as follows: in Section 2, the architecture of the proposed PMU is discussed. The design considerations of the proposed PMU are described in Section 3. Details of the sub-blocks of the PMU and simulation results are discussed in Section 4. Conclusion and future work is discussed in Section 5.

2. ARCHITECTURE OF THE PROPOSED PMU

The basic sub-circuits of the PMU shown in Figure 1, consists of an energy harvester, a voltage regulator, a voltage monitor, a battery backup module and a switched capacitor

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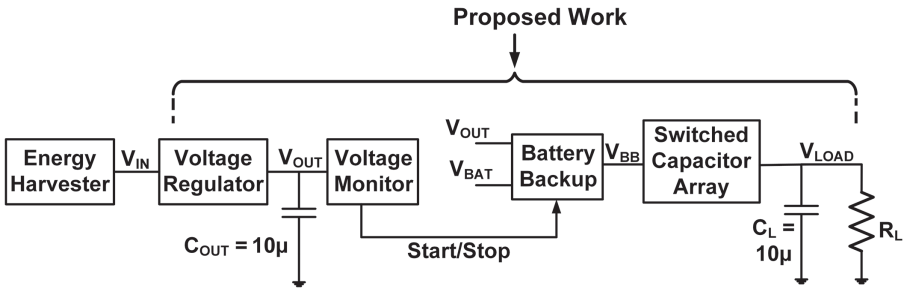

Fig. 1. Block diagram of the proposed PMU.

DC–DC converter array with a load resistor and a capacitor. The circuit diagram of the PMU shown in Figure 2 has an input voltage V_{IN} from the energy harvester to obtain a steady output voltage (V_{OUT}), regulated by the voltage regulator circuit. Following to this, the voltage monitor examines the regulated output voltage and ensures whether sufficient energy is available at the load circuit. When the regulator output voltage reaches above a predefined upper threshold voltage of about $0.8V_{OUT}$, the voltage monitor connects the regulator output powered by the EH source to V_{BB} node (see Fig. 2). It connects an external battery to the V_{BB} node as soon as the regulator output voltage (V_{OUT}) drops below the predefined lower threshold voltage of $0.6V_{OUT}$.

The external battery is used to deliver the energy to the load circuit in case the harvesting source is not available or unable to supply the required voltage for the load. The voltage monitor provides a Start/Stop condition that enables the switching of the regulated voltage or the battery voltage at the V_{BB} node, thus ensuring steady voltage supply of about 1 V. In the proposed design, the battery voltage is taken as 1 V as obtained the regulated voltage is of 1 V. Furthermore, five DC–DC step down switched capacitor converters are employed, namely 3:2, 2:1, 3:1, 4:1, 5:1 to down convert the voltage of the V_{BB} node to approximately 0.67 V, 0.5 V, 0.33 V, 0.25 V and 0.2 V, respectively. By doing this, the PMU circuit provides different supply voltages for the operation of the circuits at near threshold and subthreshold voltages in addition to operation of circuits at nominal voltages.

The two series connected solar cells provides the primary input voltage to the PMU is shown in the Figure 3. The circuit model of the solar cells[15] is specified with an open circuit voltage V_{OC} of 1.76 V and a short circuit current I_{SC} of 1 mA with 1.29 mW of maximum power.

3. DESIGN CONSIDERATIONS

The circuit is designed in the subthreshold region of MOSFET leading to low power consumption of the PMU. The subthreshold circuits in proportional to absolute temperature (PTAT) current reference,[16] reference voltage block and the error amplifier are designed in the subthreshold region. Further to this, the error amplifier is also used as a comparator in the voltage monitor. Conditions given below provides a method to design the proposed sub-circuits for $|V_{TH}| > |V_{GS}|$ and $|V_{DS}| \geq 100$ mV.

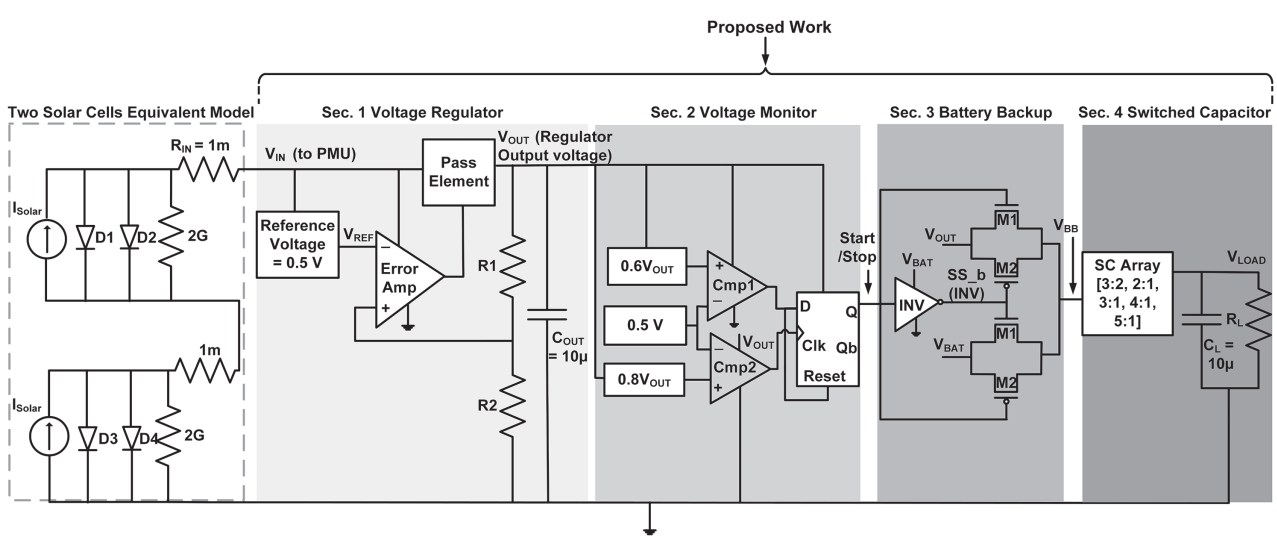

Fig. 2. Circuit diagram of the proposed work.

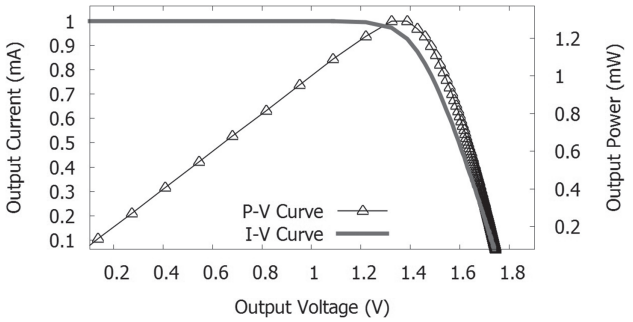

Fig. 3. Characteristics of solar cells.

The drain current[17] of MOSFET is given by:

$$I_D = I_0 \frac{W}{L}(e^{|V_{GS}|-|V_{TH}|/\eta V_T})(1 - e^{-|V_{DS}|/V_T}) \quad (1)$$

Equating $(1 - e^{-|V_{DS}|/V_T}) \equiv 1$, Eq. (1) simplifies to:

$$I_D = I_0 \frac{W}{L}(e^{|V_{GS}|-|V_{TH}|/\eta V_T}) \quad (2)$$

where, I_0 is the off current and is given by:

$$I_0 = 2 \times \mu C_{ox} \times \eta \times {V_T}^2 \quad (3)$$

where, $|V_{GS}|$ is the gate to source and $|V_{DS}|$ is the drain to source voltage. The subthreshold slope parameter η[17] is in the range between 1 to 2 and μC_{ox} is a technology dependent parameter. The ratio W/L represents the aspect ratio of the MOSFET, $|V_{TH}|$ is the threshold voltage of the MOS transistor and V_T indicates the thermal voltage.

The output resistance and the transconductance is given by:

$$R_{out} = \frac{\eta V_T}{\lambda I_D}; \quad g_m = \frac{I_D}{\eta V_T} \quad (4)$$

where, λ indicates the channel length modulation parameter.

The error amplifier shown in Figure 2, is designed where the gain ${A_V}$[18] is:

$$A_V = R_{eq} \times g_{meq} \quad (5)$$

where, R_{eq} is the equivalent output resistance and g_{meq} is the transconductance of the error amplifier.

Switched Capacitor converters are characterized by their switching frequency parameter, where the switching frequency (f) of a SC network is:

$$f = \frac{1}{R \times C} \quad (6)$$

where, R is the resistance and C is capacitance of the SC network, respectively.

The transmission gates (TG) pass '0' and '1' and are often used as MOS switches for SC converters, where the resistance Rn and Rp of the TG[19] is given by parallel combination:

$$R = (Rn \| Rp) \quad (7)$$

where, $Rn(Rp)$ is the resistance of NMOS (PMOS) switch of the TG and is given by:

$$Rn(Rp) = \frac{1}{\mu C_{ox} \times (W/L) \times (|V_{GS}| - |V_{TH}|)} \quad (8)$$

In the proposed design, a switching frequency of 13.4 kHz is attained when the resistance and the capacitance of the SC network are selected as 10 pF and 7.46 MΩ, respectively. We have adopted the approach cited in Ref. [20], where the effectiveness of a large sized flying capacitor with reduction in power loss is already discussed with slight increase in the area. We have chosen the flying capacitor C to be of 10 pF. Resistance of 7.46 MΩ is achieved by Eq. (7), Eq. (8) and the model parameters listed in the Table I.

The efficiency (η) of the PMU is the function of total output power and total input power and is given by:

$$\eta = \frac{P_{OUT}}{P_{IN}} \times 100\% = \frac{I_{OUT} \times V_{OUT}}{V_{IN} \times I_{IN}} \times 100\% \quad (9)$$

where, P_{OUT} and P_{IN} are the output and input power, V_{OUT} and V_{IN} are output and input voltage, I_{OUT} and I_{IN} are output and input current respectively.

The aspect ratios of the transistors of the sub-circuits are found out with the use of the above listed equations as well as the technology model parameters provided in Table I. In the design, a 1 nA PTAT current reference biasing circuit is designed with the use of drain current Eq. (2). Afterwards, a 2 nA and a 3 nA current references are designed using the 1 nA PTAT current reference by changing only the resistance value in the current reference.[16] The reference voltage for the error amplifier is designed using the PTAT current reference and a diode connected MOS transistor. Bias voltages for the error amplifier are designed with the help of the PTAT current reference. The error amplifier is designed with the use of bias currents, bias voltages and gain parameter using Eq. (5). For the voltage monitor, the same error amplifier is used as a comparator. Battery backup module is realized by adopting a thresholding criterion between the harvesting source and battery voltage to be connected to the V_{BB} node. The Start/Stop condition generated by the voltage monitor is triggered by a thresholding logic. The switched capacitor converters are designed at certain desired switching frequencies given by Eq. (6). The sub-circuits of the PMU are discussed in the following section.

Table I. Technology model parameters.

Parameter	PMOS	NMOS
Threshold voltage of MOSFET, V_{th}	−518 mV	461 mV
Technology dependent parameter, $k(\mu C_{ox})$	62.5 μA/V^2	316 μA/V^2
Subthreshold slope parameter, η	1.6	1.4
Channel length modulation parameter, λ	−0.95 V^{-1}	0.92 V^{-1}

4. SUB-CIRCUITS OF THE PMU

4.1. Voltage Regulator

As shown in Figure 2, the voltage regulator circuit consists of a pass element, a reference voltage, a voltage divider, an error amplifier and an output capacitor (C_{OUT}) that converts the harvested voltage into a stable voltage. In order to have a controlled voltage, the error amplifier compares the reference voltage with a sampled voltage from the resistor divider. It also regulates the current through the pass element in such a manner that the current through the pass element should increase when the output voltage (V_{OUT}) decreases and vice versa. The resistances $R1$ and $R2$ provide variable resistance and adjust the resistor divider network regularly to keep the output voltage at a constant voltage. The V_{OUT} is given by:

$$V_{OUT} = V_{REF}\left[1+\left(\frac{R1}{R2}\right)\right] \tag{10}$$

The subthreshold error amplifier has a 46.39 dB gain and unity gain bandwidth (UGBW) of 206 kHz and operates at subthreshold voltages.[21]

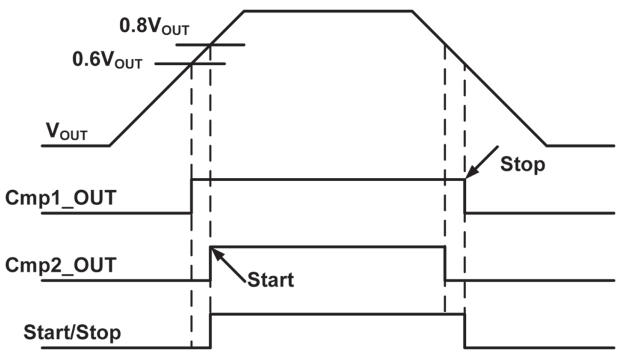

Fig. 4. Ideal response of the voltage monitor.

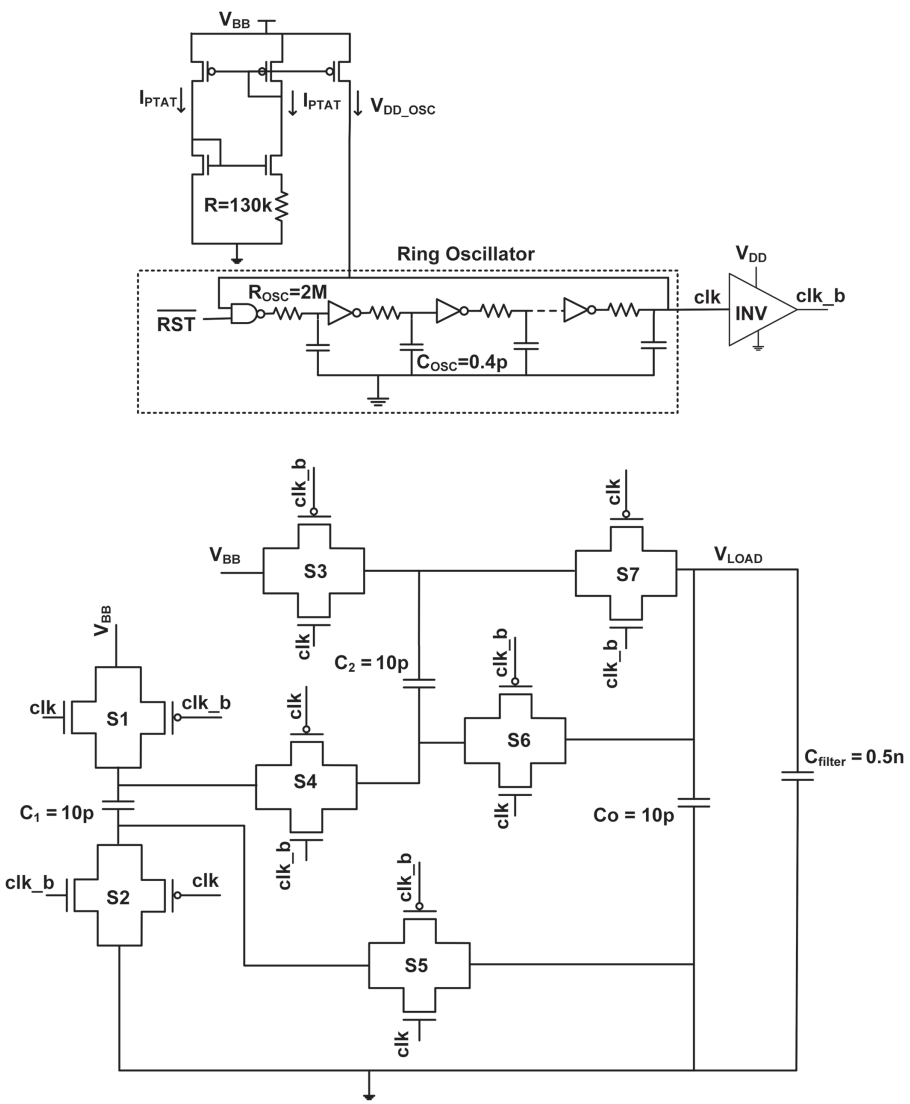

Fig. 5. Circuit diagram of 3:2 switched capacitor converter.

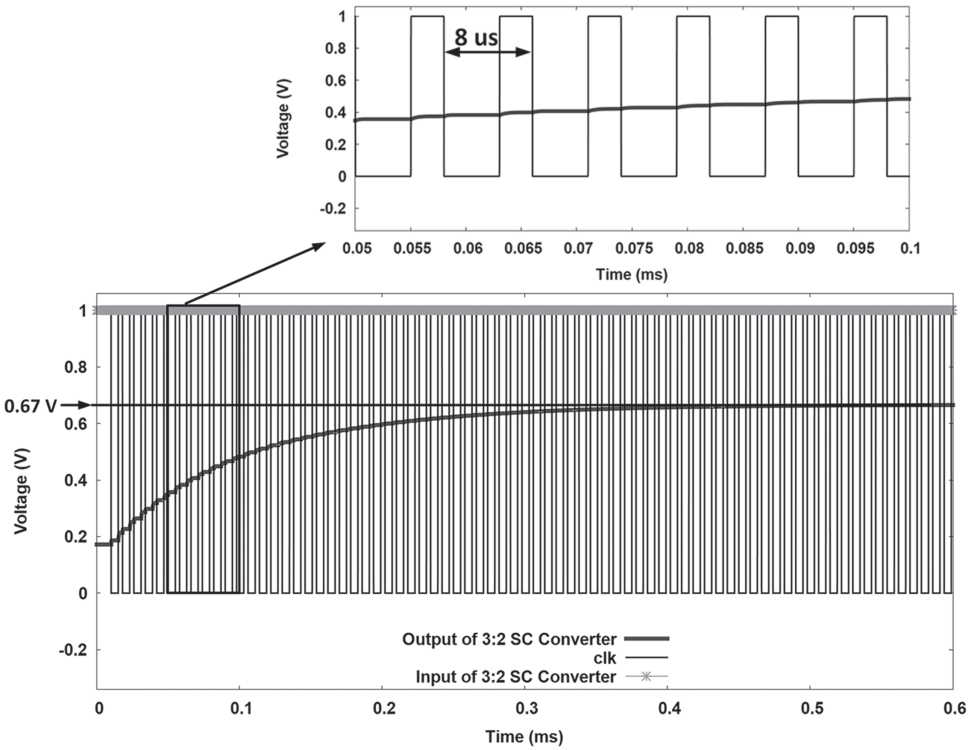

Fig. 6. Transient response of 3:2 switched capacitor converter.

4.2. Voltage Monitor

The voltage monitor[7] checks the regulator output voltage and produces a Start/Stop condition to enable the V_{OUT} or the battery voltage at the V_{BB} node (output of battery extender) with the use of two comparators and an active low reset DFF (D flip-flop) and is shown in Figure 2.

The operation of the voltage monitor is based on two voltages $0.8V_{OUT}$ and $0.6V_{OUT}$ are of provided to define upper and lower threshold voltages. When the regulator output voltage is above $0.8V_{OUT}$ (upper threshold), the Start/Stop signal is enabled, indicating the regulator output voltage to be sufficient for the load circuit. In this case, the voltage monitor connects the V_{OUT} to the V_{BB} node. The voltage monitor decouples the V_{OUT} to the output of the battery extender and connects an external battery to the V_{BB} node when the V_{OUT} becomes less than $0.6V_{OUT}$ (lower threshold), when the Start/Stop signal is disabled and is shown in Figure 4.

4.3. Battery Extender

When the harvesting source is unable to deliver the required power to the load circuit, a battery extender module is needed to ensure a reliable operation by providing regulated voltage from the battery.

Since the proposed regulator regulates the output voltage between 0.95 V and 0.968 V, we have connected a 1.0 V battery at the other terminal of the battery extender circuit. The choice of 1 V voltage supply is adequate for many low voltage, low power applications.

4.4. DC–DC Switched Capacitor Converters

A switched capacitor converter network also acts as a power converter to obtain several voltages from a single voltage.[22] In the proposed SC network, the control and distribution of charge[11] is accomplished with the help of a few switches and capacitors. The step down DC–DC converters 3:2, 2:1, 3:1, 4:1 and 5:1 are designed to regulate the PMU voltage to 0.67 V, 0.5 V, 0.33 V, 0.25 V and 0.2 V, respectively. Currently, the SC network operates in standalone mode as the control logic for automatic selection is not implemented. Such controllers are necessary for voltage dithering applications.[23]

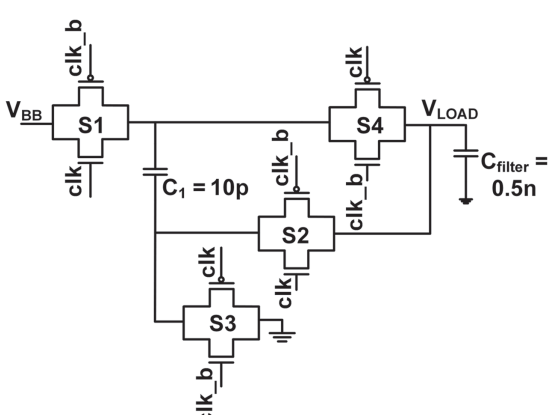

Fig. 7. Circuit diagram of 2:1 switched capacitor converter.

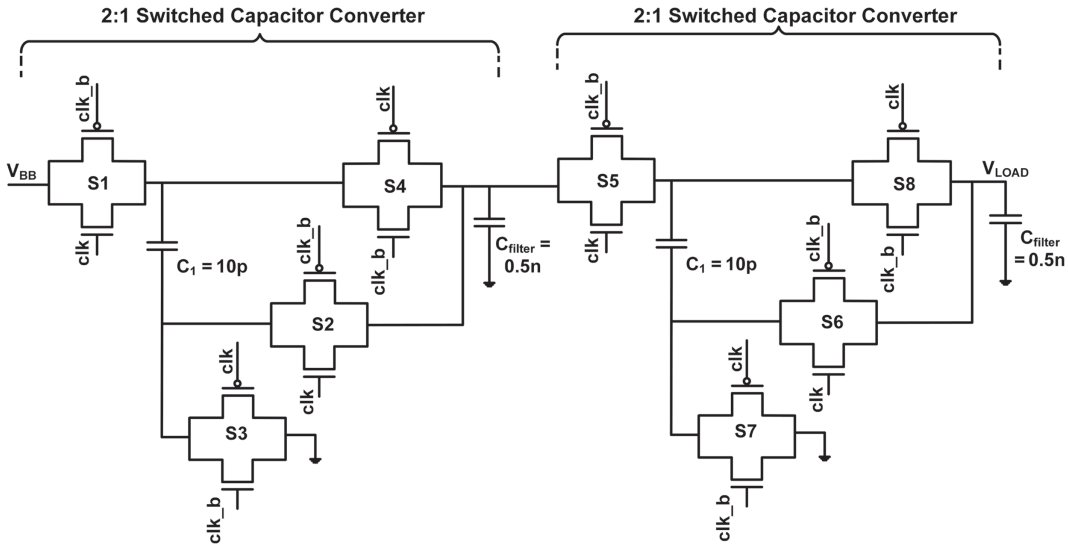

Fig. 8. Circuit diagram of 4:1 switched capacitor converter.

A clock for the SC converter is supplied by means of an RC stage ring oscillator shown in Figure 5, where the supply current to the ring oscillator is controlled by a PTAT current reference.[24] This ensures a low power operation at a lower switching frequency of 125 kHz. The SC network requires a few clock latency to produce a stable output. To minimize the voltage fluctuations at the converter output, filtering capacitor C_{filter}, is used at the output node V_{LOAD}. The working of the SC converter is described below. According to the clk, the SC converters operate in two phases:

- Phase 1—when the clk signal is at logic high and *clk_b* (complementary clk) signal goes to logic low.
- Phase 2—when clk signal becomes low and *clk_b* is at the logic high level (see Fig. 5).

4.4.1. Switched Capacitor 3:2 Converter

A 3:2 SC network comprises of switches S1 to S7 and capacitors C_{filter}, Co, C_1 and C_2 is shown in Figure 5. During Phase 1, the switches S1, S3, S5, and S6 are turned on and the parallel combination of C_1 and C_2 ($C_1||C_2$) is in series with Co producing an output voltage equal to $2/3\times$ of the input voltage (V_{BB}). The capacitors are assumed to be of same value i.e., $C_1 = C_2 = Co$. During Phase 2, the switches S2, S4, and S7 are turned on, enabling the series combination of C_1 and C_2 in parallel with Co. It results in an output voltage of $2/3\times$ its input voltage provided $C_1 = C_2 = Co$.

The transient response of the 3:2 converter is shown in Figure 6. The clk frequency is $1/8\mu s = 125$ kHz, is derived by formula $f_{\text{CLK}} = 1/(2 \times N \times C_{\text{OSC}} \times R_{\text{OSC}})$, where, N is the number of RC stage, R_{OSC} and C_{OSC} are the resistance and capacitance of the ring oscillator. To achieve 125 kHz clk frequency the values of R_{OSC}, C_{OSC} and N are kept as 2 MΩ, 0.4 pF and 5, respectively. As can be seen, the output voltage (V_{LOAD}) is down converted to 0.67 V when the input voltage (V_{BB}) of 1 V is applied. The power consumption of the 3:2 SC converter is found out to be 748 nW.

4.4.2. Switched Capacitor 2:1 and 4:1 Converters

The second switched capacitor is shown in Figure 7, is a 2:1 converter and is made up of switches S1 to S4, capacitors C_{filter} and C_1. When Phase 1 is conducting, switches S1 and S2 become active so that C_1 capacitor is placed between the input (V_{BB}) and the output node (V_{LOAD}). Switches S3 and S4 are enabled during Phase 2, where C_1 is connected between the output node V_{LOAD} and the ground, which conveys the stored charge on C_1 during the earlier cycle at the output. The 4:1 switched capacitor converter is implemented by cascading two 2:1 SC converters, as shown in Figure 8. The transient response of the 2:1 and 4:1 SC converters is shown in Figure 9. It is concluded that the load voltage is down converted to 0.5 V and 0.25 V from the input voltage of 1 V (V_{BB}) which is half and 1/4th the input voltage of 1 V. The 2:1 and 4:1 SC converters consume 751 nW and 782 nW power respectively.

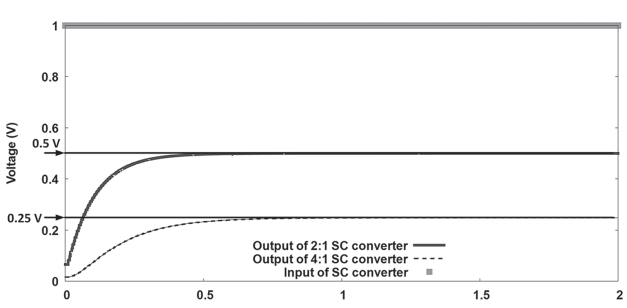

Fig. 9. Transient response of 2:1 and 4:1 switched capacitor converters.

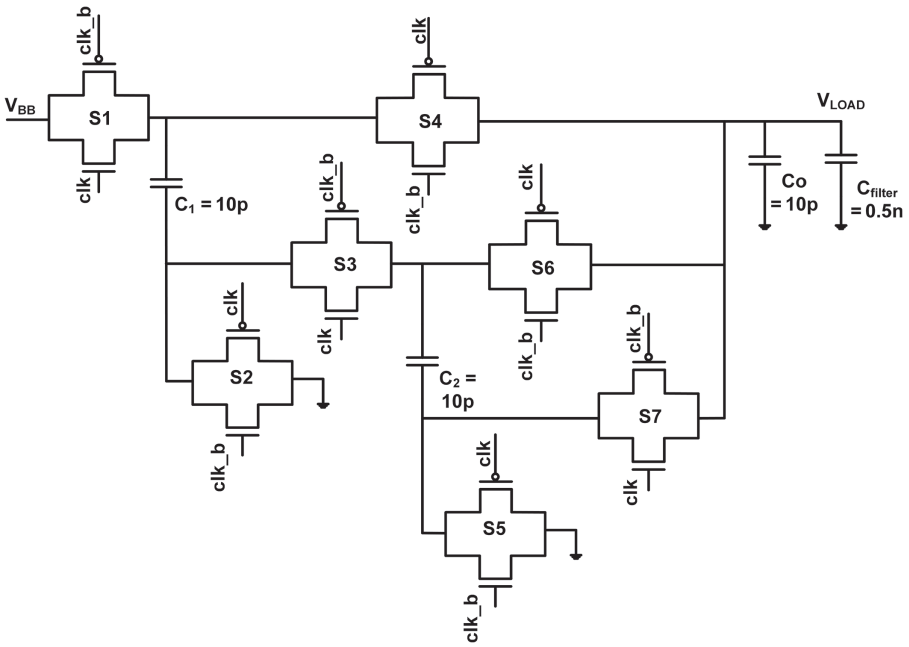

Fig. 10. Circuit diagram of 3:1 switched capacitor converter.

4.4.3. Switched Capacitor 3:1 and 5:1 Converters

The circuit diagram of the 3:1 switched capacitor converter is shown in Figure 10. It consists of switches S1 to S7 and C_1, C_2, Co and C_{filter} capacitors. The 3:1 converter operates as follows: During Phase 1, switches S1, S3 and S7 are active and thus, capacitors C_1, C_2, Co are in series. Therefore, the voltage on the input node is equally distributed to all the three capacitors assuming that $C_1 = C_2 = Co$. Hence, the voltage at capacitor Co is equal to the $1/3\times$ of the input voltage. In Phase 2, switches S2, S4, S5 and S6 are enabled and capacitors C_1, C_2, Co are in parallel between the output node (V_{LOAD}) and ground. During this Phase, C_1, C_2, Co possess equal voltage and is again $1/3$ of the input voltage. Thus, the voltage (V_{LOAD}) across the capacitor Co is $1/3$ of the input voltage V_{BB}.

The circuit diagram of a 5:1 switched capacitor converter is shown in Figure 11. As can be seen, during Phase 1, switches S1, S3, S5, S6 and S10 are ON and the equivalent circuit is shown in Figure 12(a). C_3 and Co are in series is in parallel with C_2 capacitor. Furthermore, the equivalent capacitance of C_2, C_3 and Co are in series with C_1. If $C_1 = C_2 = C_3 = Co = C$, then the

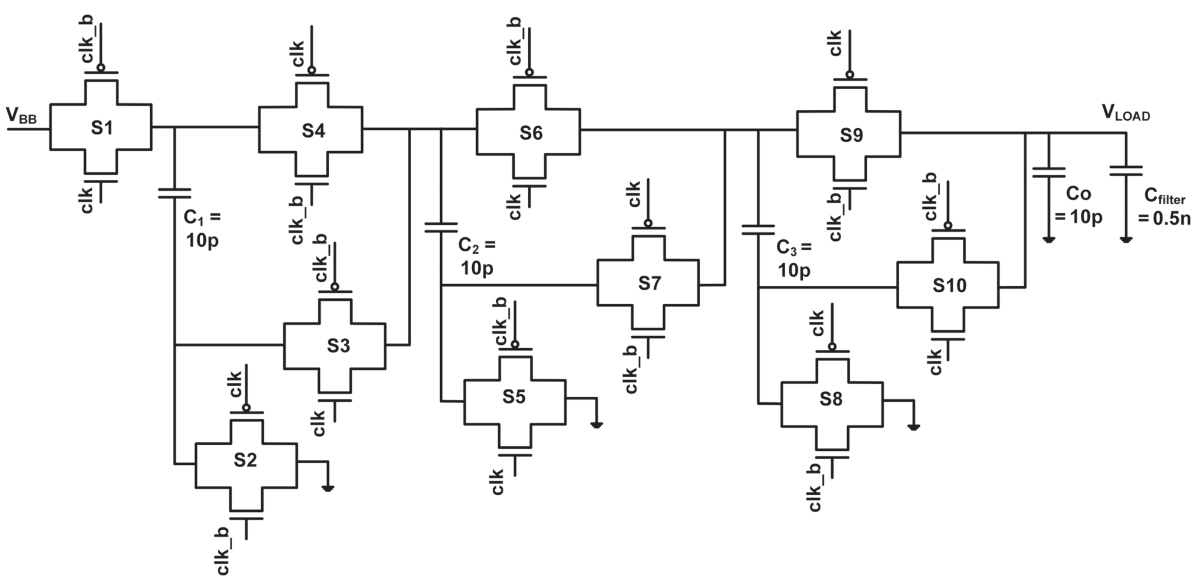

Fig. 11. Circuit diagram of 5:1 switched capacitor converter.

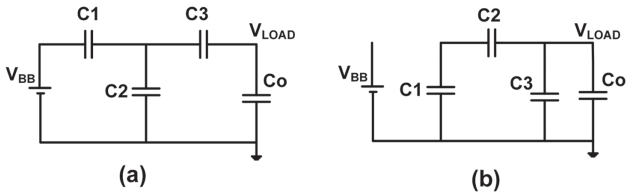

Fig. 12. Equivalent circuit for (a) phase 1 (b) phase 2 of 5:1 switched capacitor converter.

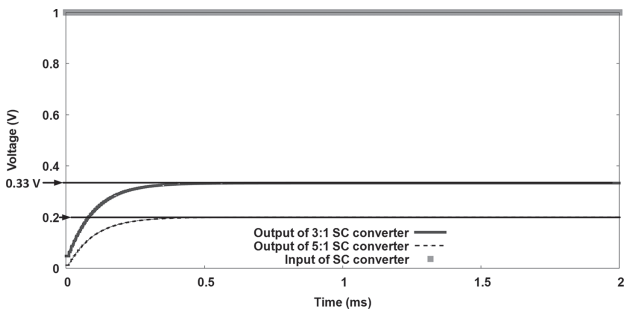

Fig. 13. Transient response of 3:1 and 5:1 switched capacitor converters.

equivalent capacitance of C_1, C_2, C_3 and Co is $3C/5$. According to the equation, $Q = C \times V$, the total charge Q will be $3C/5 \times V_{BB}$ and the charge across the capacitance Co (Qo) is $C/5 \times V_{BB}$. Therefore, the voltage across $V_{LOAD} = Qo/C = 1/5 \times V_{BB}$. Similarly, during Phase 2 the voltage across the capacitor Co is equal to the 1/5 times of the input voltage (V_{BB}).

Figure 13 shows the transient response of the 3:1 and 5:1 SC converters, that demonstrates the output voltage is down converted to 0.33 V and 0.2 V from the input voltage of 1 V. The 3:1 and 5:1 SC converters consume 818 nW and 752 nW power respectively.

4.5. Simulation Results

Different sub-blocks of the PMU are verified using 0.18 μm CMOS technology files in Cadence Virtuoso Spectre Analog Design Environment (ADE), with a load capacitor of 10 μF that seems adequate for many low power applications. To examine the upper and lower bound of the PMU, simulations are performed for two distinct values of input current:

Input current $I_{Solar} = 70$ nA (lower bound): When the input current I_{Solar} is at 70 nA, input voltage $V_{IN} = 0.98$ V and a regulated voltage $V_{OUT} = 0.95$ V is obtained.

Input current $I_{Solar} \sim 1$ mA (upper bound). For the higher input current at 1 mA, input voltage $V_{IN} = 1.33$ V and output voltage $V_{OUT} = 0.968$ V is observed.

The different sub-blocks of the PMU are verified individually and their current and power consumption is given in Table II. It should be noted that when the PMU is subjected to a higher value of input current ($\sim$1 mA), approximately 3.905 μA current is consumed by the PMU and the remaining current is available at the load resistor R_L. Based on the Eq. (9), the maximum efficiency of 72.3% is obtained for the proposed PMU at the input voltage of 1.33 V, without the power consumption of the SC converters.

In Table II, current and power consumption for the different sub-blocks of the PMU is given for two different input voltages at 0.98 V and 1.33 V. It is found that the PMU consumes a total of 3.905 μA current and 3.919 μW of power at an input voltage of 1.33 V.

The proposed PMU is compared with the reported research in literature as shown Table III, in terms of the regulated voltage, load current and power dissipation targeted for low voltage, low power applications. The few sub-circuits of the proposed PMU are designed in the subthreshold operating region, in which circuit operates on very low current. Usually, operational amplifier consumes more power compared to other circuit blocks in mixed signal design approach. Therefore, the amplifier is designed in sub-threshold region which primarily contributes to achieve low power consumption. Also, the current consumption of the ring oscillator is controlled by

Table II. Current and power consumption of the PMU sub-blocks.

Block	Sub-blocks	Current (@ 0.98 V)	Power (@ 0.98 V)	Current (@ 1.33 V)	Power (@ 1.33 V)
Voltage regulator	Error amplifier	11.8 nA	11.2 nW	14.7 nA	20 nW
	Reference voltage	2.56 nA	2.43 nW	2.9 nA	4 nW
	Voltage divider	0.84 nA	0.8 nW	0.97 nA	1.3 nW
	Pass element	1.5 pA	1.43 pW	2 pA	2.7 pW
Voltage monitor	Two comparators	21.8 nA	20.7 nW	22.15 nA	29.5 nW
	DFF	10.16 pA	9.65 pW	10.32 pA	13.7 pW
Battery backup	–	10 nA	10 nW	12 nA	12 nW
@ PMU (without SC converters)	–	48 nA*	46 nW	54 nA*	68 nW
SC converters	3:2, 2:1,	–	–	748 nA/751 nA	748 nW/751 nW
	3:1, 4:1,	–	–	818 nA/782 nA	818 nW/782 nW
	5;1 converters	–	–	752 nA	752 nW
Total	–	48 nA	46 nW	3.905 μA	3.919 μW

Notes: *1 nA current is consumed in insulator resistor kept in parallel to C_{OUT} to obtain low leakage current through the C_{OUT}. Therefore, the PMU consumes total 48 nA and 54 nA at 0.98 V and 1.33 V, respectively.

Table III. Performance comparison with reported research in literature.

Parameter	This work: @V_{IN} = 0.98 V and @I_{Solar} = 70 nA	This work: @V_{IN} = 1.33 V and @I_{Solar} = 1 mA	[5]	[6]	[7]	[8]	[9]	[25]
Regulated voltage	0.95 V	0.968 V	1.8 V	1.0 V	1.8 V	1.4 V	1.2 V, 0.5, V Variable	NA[#]
Power dissipation	46 nW	3.919 μW	1.18 μW	$\leq 2\mu$W	655 nW	2.62 μW	6.45 μW	50 nW[*]
Load current	32 nA	1.0 mA	$\geq$1 mA	NR[ϕ]	Upto 25 mA	5 μA	100 μA	NA[#]
DC–DC converter topology	–	3:2, 2:1, 3:1, 4:1, and 5:1 SC	9-Stage Step Up Charge Pump	Single Inductor Boost Converter	–	4-Stage Step Up Charge Pump	A Boost SIMO Converter	–
Technology	0.18 μm		0.18 μm	0.13 μm	0.18 μm	0.13 μm	0.13 μm	65 nm
Operating region	Subthreshold and Strong inversion		Strong inversion	Strong inversion	Sub-threshold	Strong inversion	Strong inversion	Sub-threshold

Notes: *[25] has 50 nW consumption for voltage monitor solely. #Not applicable. ϕNot reported.

PTAT current reference which leads to further reduction in power consumption. As can be seen, the proposed PMU has a power consumption of 46 nW for voltage monitor, voltage regulator and battery backup module. With the SC converters, the power consumption is 3.919 μW and is comparable to similar reported research.[5–9,25] The proposed SC converters have an added advantage of providing multiple voltages often a requirement for low voltage, low power circuits.

5. CONCLUSION AND FUTURE WORK

In this paper, a low power PMU is presented which is designed to enable energy autonomy in electronic circuits. In the proposed PMU, voltage regulation at 0.95 V and 0.968 V is achieved with input voltages of 0.98 V and 1.33 V, respectively. The maximum current that can be delivered to the load is 1 mA. The power consumed by the PMU alone is 46 nW, where SC converters are not employed. At higher voltage 1.33 V, the switched capacitor converter array provides multiple voltages but consume additional power of 3.919 μW. Battery extender module is designed for reliable operation when the circuit is expected to be powered by energy harvesters. The output voltage is regulated at 0.67 V, 0.5 V, 0.33 V, 0.25 V and 0.2 V with the use of 3:2, 2:1, 3:1, 4:1 and 5:1 SC converters, respectively. With the design of SC converters, the PMU can provide six different voltages for low voltage circuits or circuits requiring voltage dithering.[23] In the proposed PMU, the SC converters consume considerably high power and can be reduced further by implementing a controller for reconfigurability for the switched capacitor array and is left as future work.

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