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A 46 nW Power Management Unit with Battery Extender for Solar Energy Harvesters Using 0.18 μm CMOS

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This work presents the design of an ultra low power (ULP) management unit to be used in conjunction with tiny solar energy harvesters (EH) providing very low power for energy autonomy in wireless sensor applications. The power management unit (PMU) is designed using 0.18 μm CMOS in subthreshold region of MOSFET for reduced power consumption and increased efficiency. A battery extender module is also implemented to obtain continuous power in the absence of energy harvesting source. The PMU achieves a maximum of 72.3% efficiency and has a response time of 5.8088 s and 13.03 ms at the input voltages of 0.98 and 1.33 V, regulating the output voltage at 0.95 V and 0.968 V, respectively. The proposed PMU consumes 46 nW and 68 nW along with the battery extender, at input voltages of 0.98 V and 1.33 V, respectively, thereby making it suitable for ultra low voltage and low power applications.

Keywords: Nanowatt PMU, ULP, Energy Harvesting, 0.18 μm CMOS.

1. INTRODUCTION

Emerging ULP applications require complete energy autonomy and often use energy harvesters,[1] where battery replacement is cumbersome. Various sources of energy harvesting are available to convert ambient energy into useful electrical power[2,3] such as solar, thermal, vibrational, RF and other methods, among which solar energy harvesting is widely used for such low power applications.

In many battery powered systems, lower input voltages are exploited using novel circuits.[4,5] This offers opportunity for ULP applications powered by energy harvesters. This is because the voltage output of many DC harvesters such as solar cells have a variable voltage output between 0.3 V to 0.5 V and are often stacked together to meet the energy budget of such ULP applications. This variable voltage can further be regulated in the range of sub 1 V with the help of charge pump[3,4,6–8] and LDOs for the standard electronic circuits to operate.[3–7] To achieve higher efficiency of these ULP circuits, it is typically designed using switched capacitor or charge pump circuits and then regulating the output voltage using very low power LDOs.[6–8] There have been numerous efforts in designing very low voltage and low power PMUs for ULP systems.[5–7] To achieve uninterrupted operation, when there is no EH source available, battery extender modules,[9–11] are enabled using control circuitry within the PMU. When EH sources provide insufficient power to load circuit due to their intermittent nature, these external batteries serve as a supply to the load circuit.

In this paper, we propose an energy harvesting PMU for solar harvesters. The proposed design of the PMU is carried out with the primary goal of low power dissipation in the PMU circuit itself along with higher efficiency. We have used a combination of low voltage subthreshold circuits and standard CMOS circuits to achieve the same. The design achieves an improvement in terms of performance, power and efficiency when compared to similar work in the literature. This paper is organized as follows: In Section 2, the architecture of the proposed system is discussed. In Section 3, the design considerations of the PMU is discussed. Section 4 discusses various blocks of the PMU. In Section 5, simulation results are discussed. In Section 6, the conclusion and future work is discussed.

2. PROPOSED ARCHITECTURE

The proposed PMU shown in Figure 1 (shaded), consists of a voltage regulator with resistors and capacitors, a voltage monitor and a battery extender circuit. The voltage regulator circuit comprises of a reference voltage block, an error amplifier, a pass element, and a resistor divider block. Regulating resistors $R1$ and $R2$ provide variable resistance and continuously adjust the voltage divider network in

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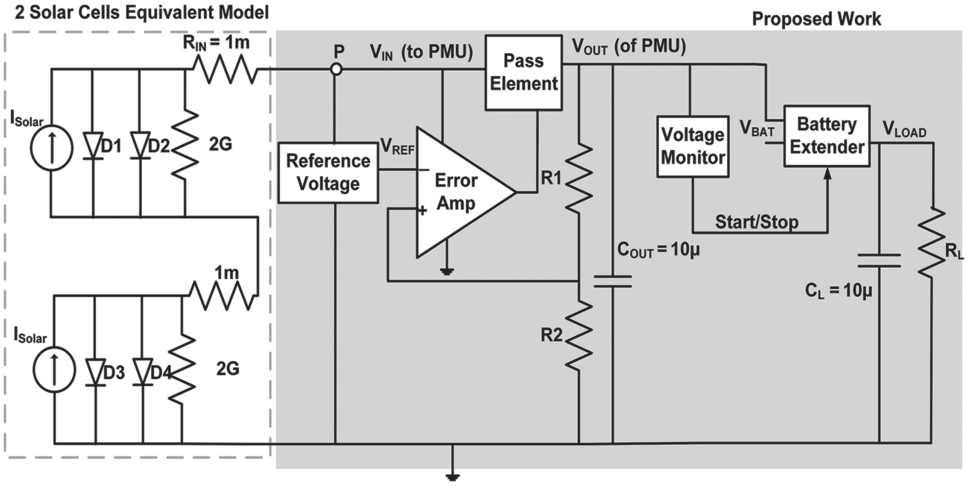

Fig. 1. Block diagram of the proposed work.

order to maintain constant voltage at the regulator output (V_{OUT}). The output voltage, across the capacitor C_{OUT} is given by:

$$V_{\mathrm{OUT}} = V_{\mathrm{REF}}\left[1+\left(\frac{R1}{R2}\right)\right] \tag{1}$$

The error amplifier compares the reference voltage V_{REF}, with the sampled voltage from the resistor divider to control the current flowing through the pass element, which further regulates the output voltage (V_{OUT}).

The voltage monitor checks whether sufficient output voltage V_{OUT}, for the load circuit is available using a comparator circuit. The comparator circuit checks as soon as the regulator output voltage decreases below an acceptable pre-defined lower threshold voltage kept at 0.6 V_{OUT} in our discussion, where the voltage monitor disconnects the load resistor R_L from the V_{OUT}. It is to be noted that the value of output capacitor C_L should be of reasonable value (typically few μF) to respond to the amplifier for ULP operation.[12] In the absence of EH source, an external battery (V_{BAT}) is used as a power supply which is a part of battery extender module. The Start/Stop signal from the voltage monitor is the control to select the power supply between EH source and external battery.

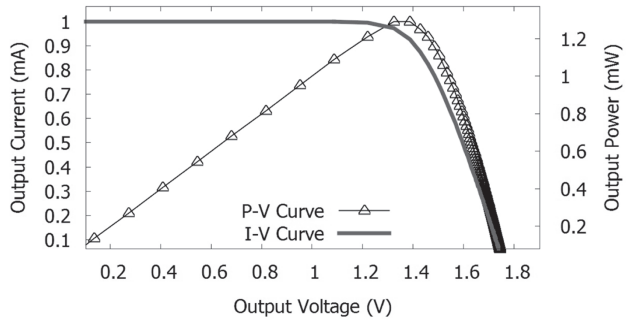

Fig. 2. I–V, P–V curves of the two series connected solar cells.

Input voltage for the PMU is generated by two series connected solar cells[13] as shown in Figure 1. The I–V and P–V characteristics of the solar cells are shown in Figure 2, where the equivalent model of solar cells is characterized by short circuit current at $I_{\mathrm{SC}} = 1$ mA and the open circuit voltage at $V_{\mathrm{OC}} = 1.76$ V. These solar cells are modeled to deliver up to 1.29 mW of maximum power to the PMU. By changing the parameters the input current and voltage can be altered.

3. DESIGN CONSIDERATIONS

To obtain low power consumption, in the proposed PMU, the voltage regulator and the voltage monitor block are operated in the subthreshold region of MOSFET with the exception of the pass element. Following conditions are therefore necessary for designing the sub-circuits: $|V_{\mathrm{TH}}| > |V_{\mathrm{GS}}|$ and $|V_{\mathrm{DS}}| \geq 100$ mV.

The drain current[14] in the subthreshold region for NMOS and PMOS is calculated as:

$$I_D = I_0\frac{W}{L}(e^{|V_{\mathrm{GS}}|-|V_{\mathrm{TH}}|/\eta V_T})(1-e^{-|V_{\mathrm{DS}}|/V_T}) \tag{2}$$

Considering $(1-e^{-|V_{\mathrm{DS}}|/V_T}) \equiv 1$, the drain current becomes,

$$I_D = I_0\frac{W}{L}(e^{|V_{\mathrm{GS}}|-|V_{\mathrm{TH}}|/\eta V_T}) \tag{3}$$

where, I_0 is the off current, given by:

$$I_0 = 2\times\mu C_{\mathrm{ox}}\times\eta\times {V_T}^2 \tag{4}$$

Table I. Model parameters.

Parameter	PMOS	NMOS
Threshold voltage, V_{th} (V)	−0.518	0.4616
Technology parameter, $k = \mu C_{\mathrm{ox}}$ (A/V^2)	0.0625 m	0.316 m
Subthreshold slope factor, η	1.6	1.4
Channel length modulation parameter, λ (V^{-1})	−0.95	0.92

where, W/L is the aspect ratio of the transistor. $|V_{GS}|$ and $|V_{DS}|$ are gate to source and drain to source voltage respectively. $|V_{TH}|$ is the threshold voltage of the MOSFET and V_T is the thermal voltage. The typical value of the subthreshold slope parameter η is in the range of $1 < \eta < 2$,[14] μ is the mobility of the carriers of the MOS devices and C_{ox} is the gate oxide capacitance.

The transconductance and the output resistance of the MOSFET in the subthreshold region is given by:

$$g_m = \frac{I_D}{\eta V_T}; \qquad R_{out} = \frac{\eta V_T}{\lambda I_D} \tag{5}$$

where, λ is the channel length modulation parameter.

As shown in Figure 7, the error amplifier compares the reference voltage with the sampled voltage.[15] The amplifier is designed with a gain parameter A_V;

$$A_V = g_{meq} \times R_{out} \tag{6}$$

where, g_{meq} is the overall transconductance and R_{out} is the equivalent output resistance of the amplifier,

$$g_{meq} = g_{m1} \times g_{m3} \tag{7}$$

$$R_{out} = (R_{o1} \parallel R_{o2}) \times R_{o3} \times R_{o4} \times R_{o5} \tag{8}$$

where, g_{m1} and g_{m3} are the transconductances of the M1 and M3 transistors and R_{o1}, R_{o2}, R_{o3}, R_{o4} and R_{o5} are the output resistances of the transistors M1, M2, M3, M4 and M5 of the error amplifier respectively as shown in Figure 7.

Further to this, Table I consists of the model parameters that are considered for the transistor dimensions to be used in the design of the sub-circuits.

Firstly, a proportional to absolute temperature (PTAT) current reference of 1 nA using drain current Eq. (3) and off current Eq. (4) is designed. The reference voltage and voltage divider circuits are designed with the help of this PTAT current reference. With the same current reference, bias voltage circuit for the error amplifier is designed. The sizing of the transistors within the amplifier is also done on the basis of bias voltages and current values. This error amplifier is further used as a comparator for the voltage monitor block discussed in the following section.

4. SUB BLOCKS OF PMU

4.1. PTAT Current Reference

In current source, the variation of the current output is proportional to the absolute temperature and the threshold voltage of a PMOS transistor is complementary to the absolute temperature (CTAT). Therefore, a PTAT current[12] is designed to counter these two effects. The PTAT is used in the regulator, voltage reference and the error amplifier. As shown in Figure 3, the PTAT consists of M1 to M10 transistors, which operate in the subthreshold region.

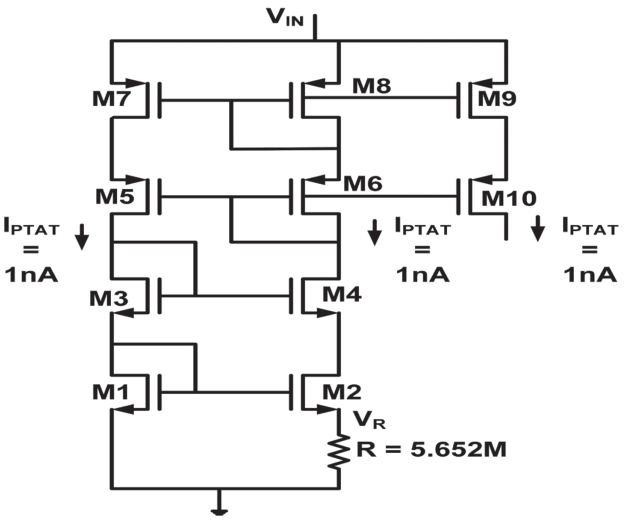

Fig. 3. Block diagram of PTAT current reference.

A small PTAT voltage V_R across the source of M2 is given as:

$$V_R = V_T \ln\left(\frac{N_2}{N_1}\right) \tag{9}$$

where, N_2/N_1 is the W/L ratio of transistors M2 and M1 respectively. The voltage V_R, in Figure 3 generates a PTAT current through the resistor R, which is used as a bias current for the reference voltage and the error amplifier, where,

$$I_{PTAT} = \frac{V_T}{R} \ln\left(\frac{N_2}{N_1}\right) \tag{10}$$

The PTAT current versus solar cells output voltage is plotted in Figure 4, to obtain the response of the PTAT current. This is because the current reference circuit is to be used in conjunction with the solar cells. As can be seen in Figure 4, the PTAT current reference generates 2.56 nA current at $V_{IN} = 0.98$ V and 2.9 nA at $V_{IN} = 1.33$ V, this input voltage (V_{IN}) to the PMU is same as the output voltage generated from the solar cells. A slight change in the PTAT current from 2.56 nA to 2.9 nA is observed with an increase in the input voltage of the PMU varying from 0.98 V to 1.33 V.

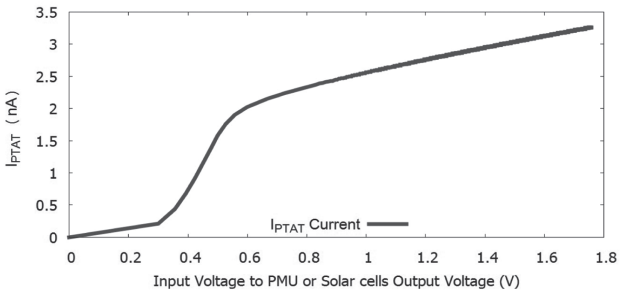

Fig. 4. PTAT reference current (nA) versus input voltage (V) of the PMU.

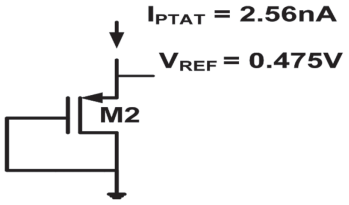

Fig. 5. Reference voltage block used for error amplifier.

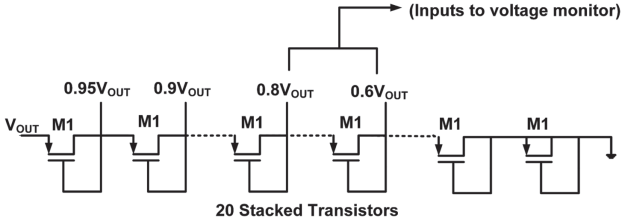

Fig. 6. Reference voltages generation for voltage monitor.

The reference voltage V_{REF}, is generated with the aid of 1 nA PTAT current reference circuit and the MOS diode, as shown in Figure 5. The V_{REF} is designed in such a way that it produces a constant voltage equal to half of the regulator output voltage. The reference voltage circuit generates 0.475 V voltage at an input voltage of $V_{IN} =$ 0.98 V from the solar cells and consumes 2.56 nA current.

As shown in Figure 6, the stacked transistors[5] are used to design reference voltages for the voltage monitor. A total of 20 sized transistors are used to divide a voltage equivalent to 50 mV at each stage. Out of the 20 different voltages that are generated, 0.8 V_{OUT} and 0.6 V_{OUT} are used at the comparator output. This further helps in the voltage monitor to generate Start and Stop conditions. Current consumption of the stacked transistors circuit is found to be 9 pA.

4.2. Error Amplifier

The two-stage operational amplifier shown in Figure 7, has a high open loop voltage gain and is achieved using cascoded gain stage.[12] The reference voltage V_{REF} is compared with the sampled voltage from the resistive divider (see Fig. 1) with the help of an error amplifier. This error amplifier also ensures that the current passing through the pass element is inversely proportional to the output voltage. To obtain ULP operation, the amplifier is designed in the subthreshold region, where the current consumption is very low and found to be 11.8 nA at $V_{IN} = 0.98$ V. The frequency response of the amplifier is shown in Figure 8 with 46.39 dB gain and unity gain bandwidth (UGBW) at 206 kHz.

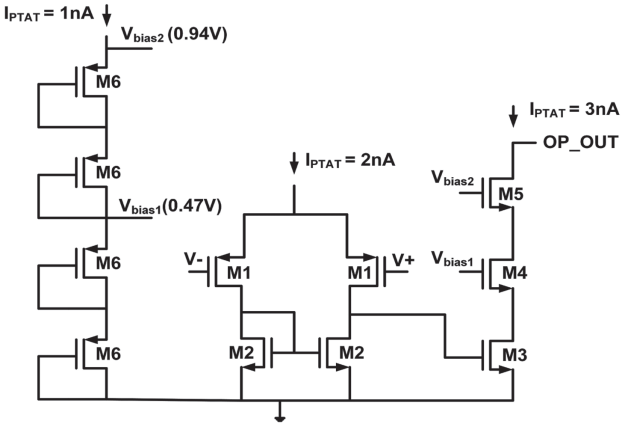

Fig. 7. Two stage operational amplifier with cascoded gain stage.

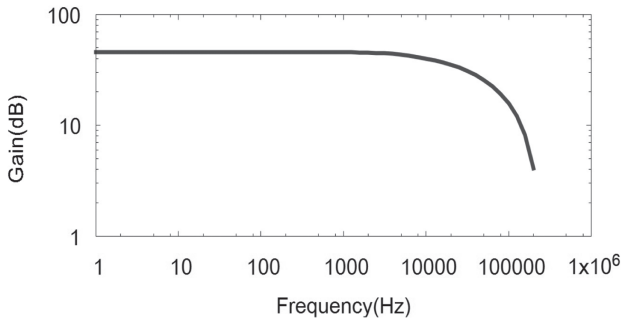

Fig. 8. Frequency response of the error amplifier.

Four diode connected MOS transistors along with 1 nA PTAT current reference are used to design, the biasing circuit for V_{bias1} and V_{bias2}, as shown in Figure 7. The bias voltages V_{bias1} and V_{bias2} are 0.47 V and 0.94 V, respectively at the input voltage (V_{IN}) of 0.98 V. By modifying the resistor R in the PTAT current reference (see Fig. 3), different I_{PTAT} currents can be obtained. In our case, this resistor R is set to be 2.77 MΩ and 1.84 MΩ to obtain 2 nA and 3 nA PTAT currents, respectively.

4.3. Pass Element and Voltage Divider

As shown in Figure 9, the pass element is used to allow the excess input current to the load from the input source. It consists of two PMOS in series, where the

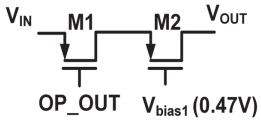

Fig. 9. Pass element for the error amplifier.

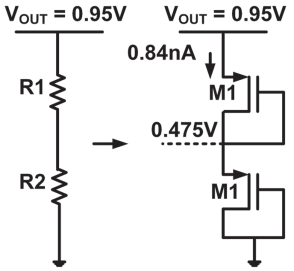

Fig. 10. Voltage divider.

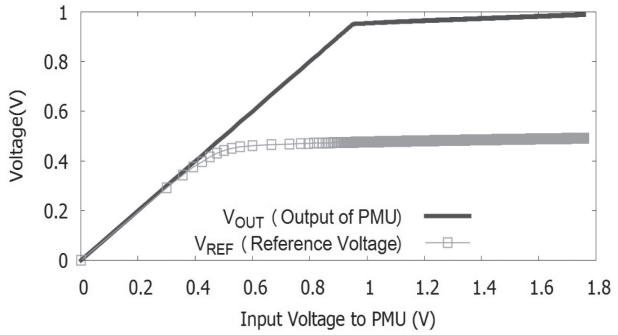

Fig. 11. Reference and output voltage of the PMU.

transistors M1 and M2 are biased with the output voltage of the error amplifier (OP_OUT) and V_{bias1}, respectively. The current delivered to the output capacitor is controlled by the pass element. For a proper operation of the PMU, the pass element is designed in the strong inversion region.[16] To accommodate the deliverable current requirement ($\sim$1 mA), the dimension of the pass element is kept at 600 μm/180 nm.

The voltage divider or the resistive divider circuit shown in Figure 10 at the output of the regulator is used to compare the output voltage V_{OUT} with the reference voltage V_{REF}. In order to divide the voltage equally across $R1$ and $R2$, the values of $R1$ and $R2$ should be equal, ensuring that V_{REF} is half the value of the V_{OUT}. These resistors are realized using diode connected MOSFETs. As shown in Figure 11, reference voltage generates 0.475 V voltage at $V_{IN} = 0.98$ V using I_{PTAT} = 2.56 nA. It is also shown that the proposed PMU regulates V_{OUT} = 0.99 V, for V_{IN} = 1.76 V in no load condition. The variation in V_{REF} when V_{IN} changes is shown in Figure 11, where a 30 mV slope is observed at V_{REF} when V_{IN} changes by 780 mV (from 0.98 V to 1.76 V).

4.4. Voltage Monitor

The voltage monitor[5] shown in Figure 12, consists of two comparators and a DFF (D flip-flop) with an active low reset. The output voltage is regulated with DFF providing the Start/Stop signal for enabling or disabling the accessibility of the PMU voltage at the load R_L. It begins to

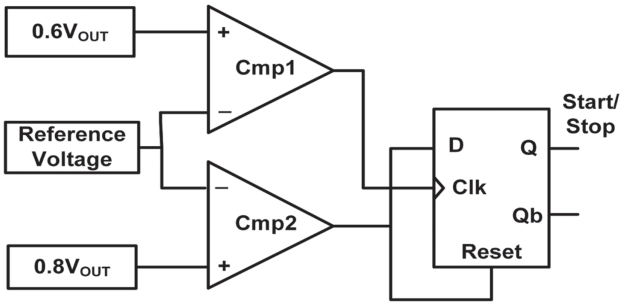

Fig. 12. Block diagram of voltage monitor.

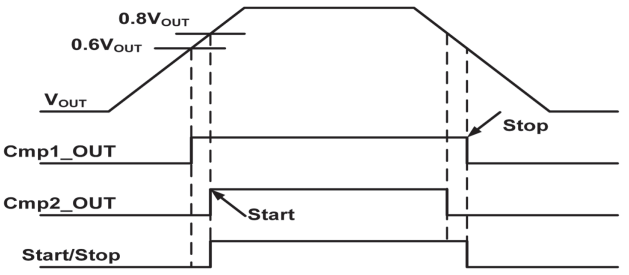

Fig. 13. Ideal response of voltage monitor.

generate the start signal at 0.76 V (=0.8 $\times$ 0.95 V) and the stop signal at 0.57 V (=0.6 $\times$ 0.95 V) as shown in Figure 13. The upper and lower threshold voltages for voltage monitor are fixed at 0.8 V_{OUT} and 0.6 V_{OUT}. The values can be altered depending on the application. The voltage monitor forces the load (say a WSN) to connect V_{OUT} to V_{LOAD}, as soon as the regulator output voltage reaches the upper threshold voltage of 0.8 V. It disconnects the load resistor R_L from the output of the regulator as soon as the regulator output voltage decreases below the lower threshold voltage of 0.6 V. Thus, reliable operation of the load is ensured by ensuring the availability of sufficient energy.

As can be seen in Figure 12, the output of first comparator Cmp1, is driven by lower threshold voltage and is connected to the clock terminal of DFF. The output of second comparator Cmp2, is driven by upper threshold voltage, and is connected to the D input and the active low reset input. The ideal response of the voltage monitor is shown in Figure 13. When the regulator output voltage becomes greater than 0.8 V (Start enabled), the output of Cmp2 goes to logic high. The output of Cmp1 will be logic low when the regulator output voltage becomes less than 0.6 V (Start disabled or Stop enabled). The voltage monitor consumes approximately 22 nA of current. Out of which, 11 nA is consumed by each comparator and 10.16 pA is consumed by the DFF.

The transient behavior of the Cmp1 is shown in Figure 14. As can be seen, when the positive terminal of the Cmp1, is at a higher voltage than 0.475 V (V_{REF}), the output Cmp1_OUT is at logic high.

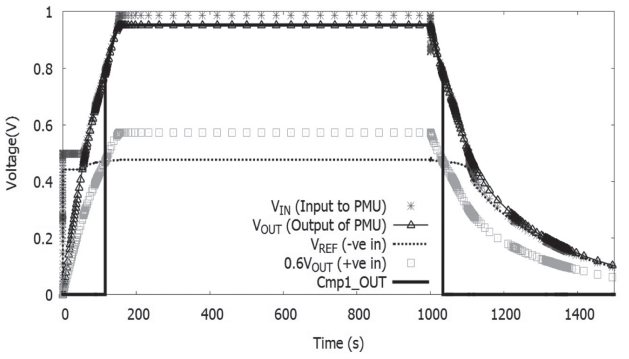

Fig. 14. Comparator output.

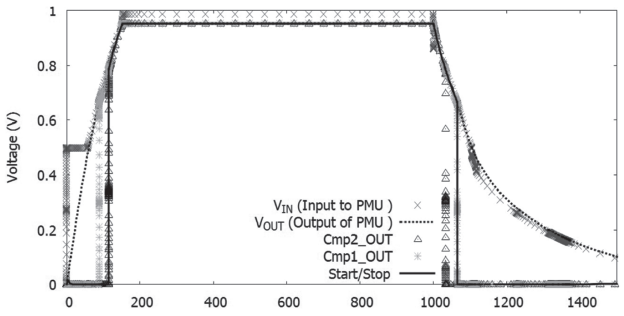

Fig. 15. Response of voltage monitor block.

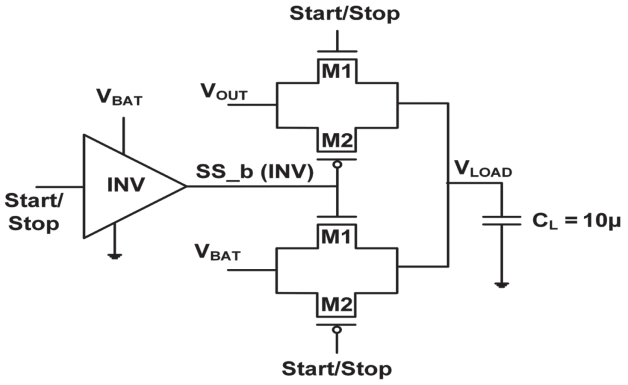

Fig. 16. Block diagram of battery extender.

The transient response of the voltage monitor is shown in Figure 15. When Cmp2_OUT goes to logic high, Start/Stop signal is enabled and is disabled as Cmp1_OUT makes a transition from high to low. The correct functionality of the voltage monitor block is ensured as the outputs of Cmp2 and Cmp1 are driven by 0.76 V ($=0.8 \times 0.95$ V) and 0.57 V ($= 0.6 \times 0.95$ V), respectively.

4.5. Battery Extender

A simple battery extender module developed in this work serves as a controller that selects an alternate power supply when EH source is absent or unable to provide sufficient energy to the load circuit. The value of 1.0 V as a battery source is arbitrarily chosen to suit our design requirements and can be varied to suit other application requirements.

A control signal (Start/Stop) enables the load to be connected to either regulator output (V_{OUT}) or external battery (V_{BAT}). It ensures that PMU will operate regardless of the presence of harvesting source and consumes 10 nA current.

When energy harvesting PMU has a voltage output (V_{OUT}) higher than 0.8 V (0.8 V_{OUT}), the load is connected to the V_{OUT} via the upper transmission gate as shown in Figure 16. In the absence of it, is connected to the external battery (V_{BAT}) of 1.0 V via the lower transmission gate.

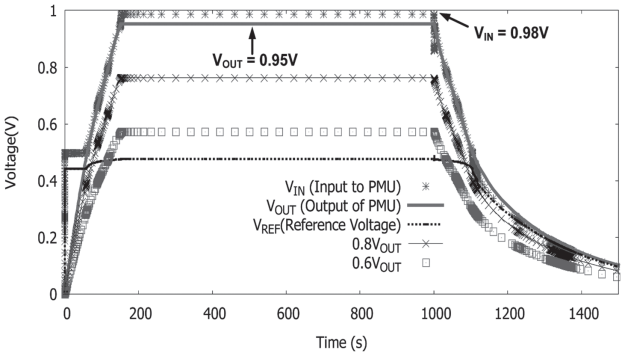

Fig. 17. Voltages used for comparison at lower input current.

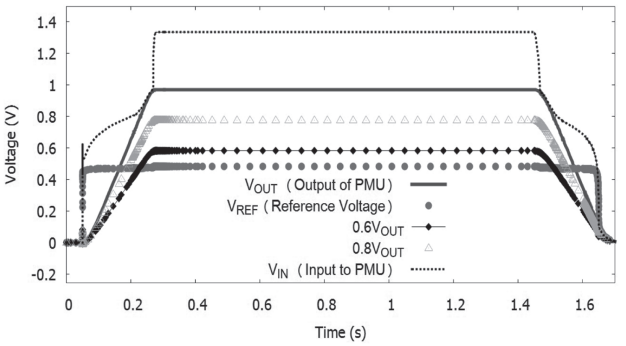

Fig. 18. Voltages used for comparison at higher input current.

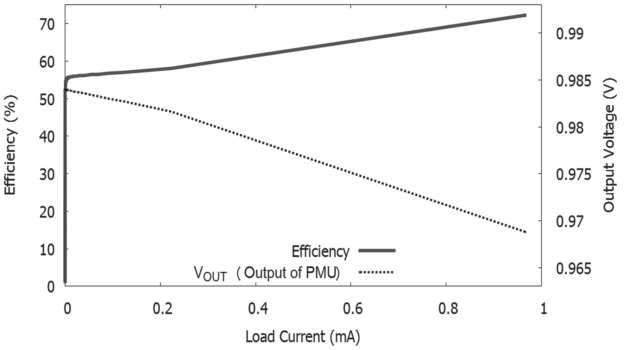

Fig. 19. Load analysis and PMU efficiency.

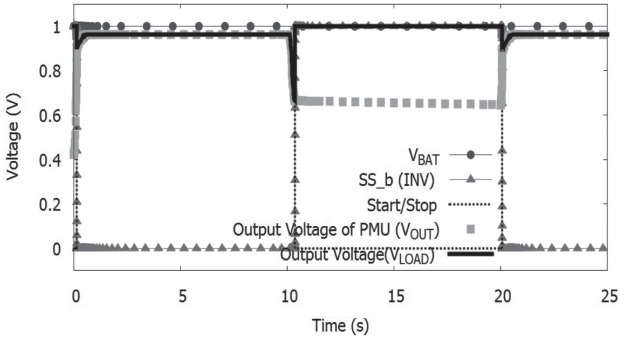

Fig. 20. Transient response of battery extender.

Table II. Power and current consumption.

Block	Sub-block	Current (A) (@ 0.98 V)	Power (W) (@ 0.98 V)	Current (A) (@ 1.33 V)	Power (W) (@ 1.33 V)
Regulator	Error amplifier	11.8 n	11.2 n	14.7 n	20 n
	Reference voltage	2.56 n	2.43 n	2.9 n	4 n
	Voltage divider	0.84 n	0.8 n	0.97 n	1.3 n
	Pass element	1.5 p	1.43 p	2 p	2.7 p
Voltage monitor	Two comparators	21.8 n	20.7 n	22.15 n	29.5 n
	DFF	10.16 p	9.65 p	10.32 p	13.7 p
@ PMU (without battery extender)*	–	38 n	36 n	42 n	56 n
Battery extender	–	10 n	10 n	12 n	12 n
Total (with battery extender)	–	48 n	46 n	54 n	68 n

Notes: *1 nA current is consumed by insulation resistor kept in parallel with output capacitor C_{OUT} to reduce leakage current through the capacitor. Hence total current consumption and power consumption of the proposed PMU becomes 38 nA and 36 nW @ 0.98 V, and 42 nA and 56 nW @ 1.33 V, respectively.

5. SIMULATION RESULTS AND DISCUSSION

The schematic simulations were carried out for different sub-blocks of the PMU, using 0.18 μm CMOS physical models. The output capacitor is chosen as 10 μF, a sufficient value for ULP WSN applications.

Two different conditions: one for low and the other for high input power are considered and discussed in the following sub-section. This demonstrates the upper and lower boundaries of the PMU operation.

5.1. Analysis for Lower Value of Input Power

Various voltages are used for comparison, in the voltage monitor is shown in Figure 17. With $I_{Solar} = 70$ nA, $V_{IN} =$ 0.98 V and the V_{OUT} = 0.95V is observed. Therefore, 0.8 V_{OUT} is equivalent to 0.76 V and 0.6 V_{OUT} is equivalent to 0.57 V. These voltages are fed to the comparator block and enable the Start/Stop signal correctly. It is observed that out of the total current passing through the circuit, 32 nA current is delivered to the R_L and 38 nA is consumed by the PMU. The propagation delay between input and output of the PMU is found to be 5.8088 s with the input current of 70 nA (this is the minimum current below which the PMU stops functioning and the voltage at the solar cell output is also minimum at 0.98 V). The power delay product (PDP) is found to be 267.2 nJ and is higher due to slower response of the PMU charging circuit at lower value of the current.

5.2. Analysis for Higher Value of Input Power

For a higher current, the simulation is carried out and is shown in Figure 18. Input voltage $V_{IN} = 1.33$ V and $V_{OUT} = 0.968$ V are obtained at the input current, $I_{Solar} \sim$ 1 mA. 42 nA of this current is consumed in the PMU and the rest is delivered to R_L. With the input current of 1 mA (@1.33 V; this is the maximum voltage output of the solar cell), propagation delay of 13.03 ms is observed. The PDP is found to be 888.04 pJ.

Figure 19 presents the maximum regulator efficiency and output voltage variation with the load current. As can be observed, the proposed PMU has a maximum efficiency of 72.3%. The PMU can also work with the higher load currents up to 1 mA. The output voltage at the load R_L is seen to be slightly decreased at a higher load current as shown in Figure 19.

The transient response of the battery extender module is shown in Figure 20. When the PMU supplies sufficient voltage at its output ($V_{OUT} = 0.968$ V) of 0.968 V (>0.77 V (=0.8 × 0.968 V)), the Start/Stop signal is enabled and V_{OUT} is available at the load circuit. The load circuit has the voltage equivalent to the V_{BAT} when V_{OUT} is below a pre-defined value of 0.58 V (=0.6 × 0.968 V).

Table III. Performance comparison to reference works.

Parameter	Proposed work		[5]	[6]	[8]	[17]*
	@ $V_{IN} = 0.98$ V and @ $I_{Solar} = 70$ nA	@ $V_{IN} = 1.33$ V and @ $I_{Solar} = 1$ mA				
Output voltage regulation (V)	0.95	0.968	1.8	1.4	1.0	NA$^{\phi}$
Power dissipation (W)	46 n	68 n	655 n	2.62 μ	256 μ	50 n
Load current (A)	32 n	1.0 m	25 m	5 μ	0.6–1.1 m	NA$^{\phi}$
Delay (s)	5.8088	13.03 m	NR$^{\#}$	NR$^{\#}$	NR$^{\#}$	6 μ
Power delay product (J)	267.2 n	888.04 p	NR$^{\#}$	NR$^{\#}$	NR$^{\#}$	0.3 p
Process	0.18 μm		0.18 μm	0.13 μm	0.18 μm	65 nm
Max. efficiency (%)	72.3		NR$^{\#}$	58	70	NA$^{\phi}$
Operating region	Subthreshold		Subthreshold	Strong inversion	Strong inversion	Subthreshold

Notes: *[17] is for voltage monitor block only. $^{\#}$Not reported. $^{\phi}$Not applicable.

The current and power consumption of individual block of the PMU for both input voltages at 0.98 V and 1.33 V are shown in Table II. The proposed PMU consumes 36 nW and 56 nW at V_{IN} = 0.98 V and V_{IN} = 1.33 V, respectively without the battery backup module. The total power consumption of the proposed work is slightly increased due to some nano watt current consumption in the battery backup module. Furthermore, Table III compares the proposed PMU with the similar works discussed in the literature. From Table III, it can be concluded that proposed PMU has comparable power consumption and efficiency with respect to the mentioned works.[5,6,8,17]

6. CONCLUSION

The proposed work presents the design of an ULP capacitive solar PMU. The proposed PMU is focused mainly on low power circuit blocks working at subthreshold voltages. All the blocks of the PMU, except the pass element are designed in subthreshold region. At the input voltage of 0.98 V, the PMU regulates the output voltage to 0.95 V with 36 nW of power consumption. For a input voltage of 1.33 V, it regulates the output voltage to 0.968 V with 56 nW power consumption and a maximum efficiency of 72.3% is achieved without the battery extender circuit. The proposed PMU possess the PDP of 267.2 nJ and 888.04 pJ at the input voltages of 0.98 and 1.33 V, respectively. The PMU consumes 46 nW and 68 nW of power at input voltages of 0.98 V and 1.33 V, respectively, when the battery extender module is in operation. This battery extender module ensures reliable power delivery to the load by switching between the EH module and V_{BAT}. The minimum voltage at which the PMU starts to operate is at 0.55 V and the regulation of the output is obtained at 0.95 V. Lower power consumption and better efficiency makes the proposed PMU viable for various applications where low voltage, low power operations are required.

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