A 36 nW Power Management Unit for Solar Energy Harvesters Using 0.18 µm CMOS

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Abstract. This work presents the design of ultra low power (ULP) management unit to be used in conjunction with tiny solar cells or energy harvesters providing very low power for wireless sensor node (WSN) applications for energy autonomy. The power management unit (PMU) is implemented using 0.18 µm CMOS in subthreshold region of MOSFET for reduced power consumption with increased efficiency. It regulates the output voltage at 0.95 V and 0.968 V when the input voltages are 0.98 V and 1.33 V, respectively and achieves maximum 72.3% efficiency. The proposed PMU consumes 36 nW and 56 nW of power, at input voltages of 0.98 V and 1.33 V, respectively, thereby making it suitable for ultra low voltage, low power applications.

Keywords: Nanowatt PMU · ULP · Energy harvesting
0.18 µm CMOS

1 Introduction

Emerging ULP applications require energy harvesters for complete energy autonomy [1], where battery replacement is cumbersome. Energy harvesting from solar, thermal, piezo, electromagnetic, RF and several other techniques exist that convert micro harvested energy to useful electrical energy [2]. Out of these, solar energy harvesting is widely adopted as it is abundantly available and is affordable with an acceptable power output, that is ideal for ULP applications. Furthermore, with several of these tiny cells together, it is possible to meet the energy budget of the ULP systems. However, it is difficult to power up the system directly from these energy harvesters and often require to undergo level conversions using low dropout (LDO) regulation circuits. Hence, power management is necessary to regulate the harvested energy or voltage in PMU circuits to get a stable power supply [3].

In many battery powered systems, lower input voltages are exploited using novel circuits [4]. This offers opportunity for ULP applications powered by energy harvesters. This is because the voltage output of many DC harvesters such as solar cells have a variable voltage output between 0.3 V to 0.5 V. This variable voltage can further be regulated in the range of sub 1 V with the help of charge pump [3,5–7] and LDOs for the standard electronic circuits to operate [3–7].

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To achieve higher efficiency of these ULP circuits, it is typically designed using switched capacitor or charge pump circuits and then regulating the output voltage using very low power LDOs [5–7]. There have been numerous efforts in designing very low voltage and low power PMUs for ULP systems [4–7].

In this paper, we propose an energy harvesting PMU for solar harvesters. The proposed design of the PMU is carried out with the primary goal of low power dissipation in the PMU circuit itself along with higher efficiency. We have used a combination of low voltage subthreshold circuits and standard CMOS circuits to achieve the same. The design achieves an improvement in terms of performance, power and efficiency when compared to similar work in the literature.

This paper is organized as follows: In Sect. 2, the architecture of the proposed system is discussed. In Sect. 3, the design considerations of the PMU is discussed. Section 4 discusses various blocks of the PMU. In Sect. 5, simutation results are discussed. In Sect. 6, the conclusion and future work is discussed.

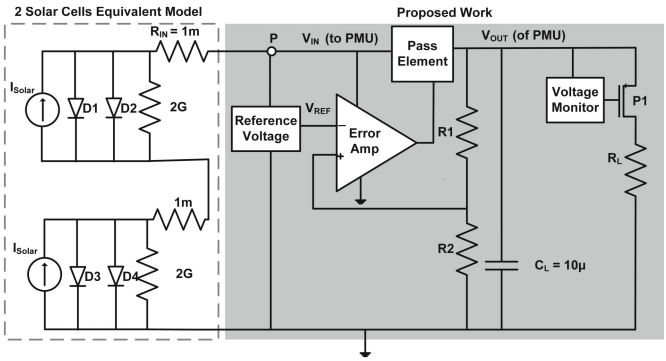


Fig. 1. Block diagram of the proposed work

2 Proposed Architecture

The proposed PMU shown in Fig. 1, consists of a voltage regulator and a voltage monitor with resistors and capacitors. The voltage regulator circuit comprises of a reference voltage block, an error amplifier, a pass element, and a resistor divider block. Regulating resistors R1 and R2 provide variable resistance and continuously adjust the voltage divider network in order to maintain constant voltage at the output (V_{OUT}). The output voltage, across the load capacitor C_L is given by:

$$V_{OUT} = V_{REF}\left[1 + \left(\frac{R1}{R2}\right)\right] \tag{1}$$

The error amplifier compares the reference voltage V_{REF}, with the sampled voltage from the resistor divider to control the current flowing through the pass element, which further regulates the output voltage (V_{OUT}).

The voltage monitor checks whether sufficient output voltage for the load circuit is available using a comparator circuit. The comparator circuit checks as soon as the regulator output voltage decreases below an acceptable pre-defined lower threshold voltage kept at $0.6V_{OUT}$ in our discussion, where the voltage monitor disconnects the load resistor R_L from the supply voltage via the switch P1. It is to be noted that the value of output capacitor C_L should be of reasonable value (typically few μF) to respond to the amplifier for ULP operation [8].

3 Design Considerations

The proposed PMU has all the blocks operated in subthreshold region, except the pass element. Following conditions are therefore necessary for designing the sub-circuits: $|V_{TH}| > |V_{GS}|$ and $|V_{DS}| \geq 100\,\text{mV}$

The drain current [9] in the subthreshold region for NMOS and PMOS is calculated as:

$$I_D = I_0 \frac{W}{L} \left(1 - e^{\frac{|V_{GS}|-|V_{TH}|}{\eta V_T}}\right) \left(1 - e^{\frac{-|V_{DS}|}{\eta V_T}}\right) \tag{2}$$

considering $\left(1 - e^{\frac{-|V_{DS}|}{\eta V_T}}\right) \equiv 1$, the drain current becomes,

$$I_D = I_0 \frac{W}{L} \left(1 - e^{\frac{|V_{GS}|-|V_{TH}|}{\eta V_T}}\right) \tag{3}$$

where, I_0 is the off current, given by:

$$I_0 = 2 \times \mu C_{ox} \times \eta \times {V_T}^2 \tag{4}$$

where, $\frac{W}{L}$ is the aspect ratio of the transistor. $|V_{GS}|$ and $|V_{DS}|$ are gate to source and drain to source voltage respectively. $|V_{TH}|$ is the threshold voltage of the MOSFET and V_T is the thermal voltage. Subthreshold slope parameter η is typically in the range $1 < \eta < 2$ [9], μ is the mobility of the carriers of the MOS devices and C_{ox} is the gate oxide capacitance.

The transconductance and the output resistance of the MOSFET in the subthreshold region is given by:

$$g_m = \frac{I_D}{\eta V_T}; \qquad R_{out} = \frac{\eta V_T}{\lambda I_D} \tag{5}$$

where, λ is the channel length modulation parameter.

As shown in Fig. 4, the error amplifier compares the reference voltage with the sampled voltage [10]. The amplifier is designed with a gain parameter A_V;

$$A_V = g_{meq} \times R_{out} \tag{6}$$

where, g_{meq} is the overall transconductance and R_{out} is the equivalent output resistance of the amplifier,

$$g_{meq} = g_{m1} \times g_{m3} \tag{7}$$

$$R_{out} = (R_{o1} \parallel R_{o2}) \times R_{o3} \times R_{o4} \times R_{o5} \tag{8}$$

where, g_{m1} and g_{m3} are the transconductances of the M1 and M3 transistors and R_{o1}, R_{o2}, R_{o3}, R_{o4} and R_{o5} are the output resistances of the transistors M1, M2, M3, M4 and M5 of the error amplifier respectively as shown in Fig. 4.

Further to this, Table 1 consists of the model parameters that are considered for the transistor dimensions to be used in the design of the sub-circuits.

Table 1. Model parameters

Parameter	PMOS	NMOS
Threshold voltage, $V_{th}(V)$	−0.518	0.4616
Technology parameter, $k = \mu C_{ox}(A/V^2)$	0.0625 m	0.316 m
Subthreshold slop factor, η	1.6	1.4
Channel length modulation parameter, $\lambda(V^{-1})$	−0.95	0.92

Firstly, a proportional to absolute temperature (PTAT) current reference of 1 nA using drain current Eq. (3) and off current Eq. (4) is designed. With the help of this current reference, reference voltage and voltage divider circuits are designed. With the same current reference, bias voltage circuit for the error amplifier is designed. The bias voltages and current values are used for the sizing of the transistors within the amplifier. This error amplifier is further used as a comparator for the voltage monitor block discussed in the following section.

4 Sub Blocks of PMU

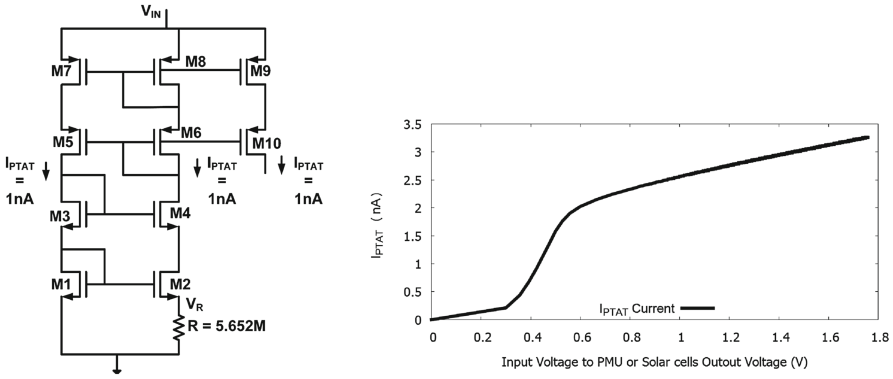
4.1 PTAT Current Reference

In current source the variation of the current output is proportional to the absolute temperature and the threshold voltage of a PMOS transistor is complementary to the absolute temperature (CTAT). Therefore, in the current reference for compensating these two effects, a PTAT current reference is designed [8]. The PTAT is used in the regulator, voltage reference and the error amplifier. As shown in Fig. 2a, the PTAT consists of M1 to M10 transistors, operating in the subthreshold region. A small PTAT voltage V_R across the source of M2 is given as:

$$V_R = V_T ln\left(\frac{N_2}{N_1}\right) \tag{9}$$

where, $\frac{N_2}{N_1}$ is the $\frac{W}{L}$ ratio of transistors M2 and M1 respectively. The voltage V_R, in Fig. 2a generates a PTAT current through the resistor R, which is used as a bias current for the reference voltage and the error amplifier, where,

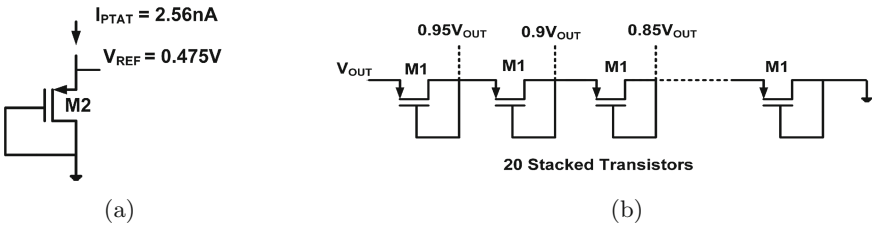
$$I_{PTAT} = \frac{V_T}{R} ln\left(\frac{N_2}{N_1}\right) \tag{10}$$



(a) (b)

Fig. 2. (a) PTAT Current Reference Block Diagram (b) PTAT Reference Current (nA) *vs.* Input Voltage (V) of the PMU

To find out the response of the PTAT circuit, the PTAT current versus solar cells output voltage is plotted in Fig. 2b. This is because the current reference circuit is to be used in conjunction with the solar cells. As can be seen in Fig. 2b, the PTAT current reference generates 2.56 nA current at $V_{IN} = 0.98$ V and 2.9 nA at $V_{IN} = 1.33$ V, this input voltage (V_{IN}) to the PMU is same as the output voltage generated from the solar cells. A slight change in the PTAT current from 2.56 nA to 2.9 nA, is observed with an increase in input voltage of the PMU from 0.98 V to 1.33 V.



(a) (b)

Fig. 3. (a) Reference Voltage Block used for Error Amplifier (b) Reference Voltages Generation for Voltage Monitor

4.2 Reference Voltage

As shown in Fig. 3a, the reference voltage V_{REF}, is generated using the 1 nA PTAT current reference circuit and the MOS diode. The V_{REF} is designed in such a way that it produces constant voltage equal to half of the regulator output voltage. As the reference voltage circuit generates 0.475 V voltage, the designed PMU regulates the output voltage to be at 0.95 V at an input voltage $V_{IN} = 0.98$ V from the solar cells. The current consumption of the reference voltage circuit is 2.56 nA.

Reference voltages for the voltage monitor are designed with the help of stacked transistors [4] as shown in Fig. 3b. A total of 20 sized transistors are used to divide a voltage equivalent to 50 mV at each stage. From the 20 different voltages that are generated, $0.8V_{OUT}$ and $0.6V_{OUT}$ are used at the comparator output. This further helps in voltage monitor to generate Start and Stop conditions. Current consumption of the designed stacked transistors circuit is found to be 9 pA.

4.3 Error Amplifier

A two-stage operational amplifier is shown in Fig. 4. The cascoded gain stage helps in achieving high open loop voltage gain [8]. The error amplifier compares the reference voltage V_{REF} with the sampled voltage from the resistive divider comprising of R1 and R2 (see Fig. 1). The error amplifier also ensures that current passing through the pass element is inversely proportional to the output voltage. To obtain ULP operation, this amplifier is designed in the subthreshold region, where the current consumption of the error amplifier is very low and found to be 11.8 nA at $V_{IN} = 0.98$ V. The frequency response of the amplifier is shown in Fig. 5 with 46.39 dB gain and unity gain bandwidth (UGB) at 206 kHz.

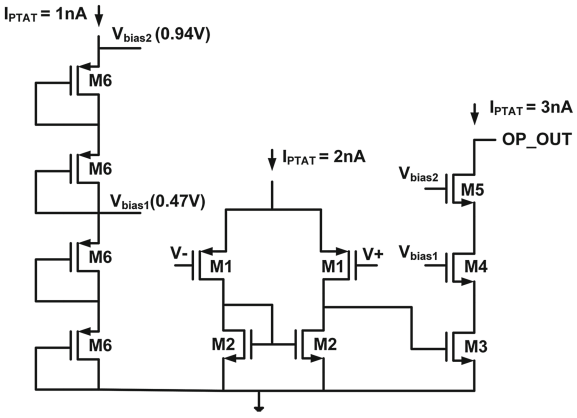


Fig. 4. Two stage operational amplifier with cascoded gain stage

The biasing circuit for V_{bias1} and V_{bias2} shown in Fig. 4, is designed with the help of four diode connected MOS transistors and the 1 nA PTAT current reference. The bias voltages V_{bias1} and V_{bias2} are 0.47 V and 0.94 V, respectively at the input voltage (V_{IN}) of 0.98 V. By modifying the resistor R in the PTAT current reference (see Fig. 2a), different I_{PTAT} currents can be obtained. In our case, this resistor R is set to be 2.77 MΩ and 1.84 MΩ to obtain 2 nA and 3 nA PTAT currents, respectively.

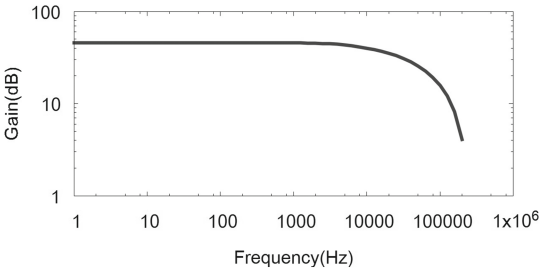


Fig. 5. Frequency response of the error amplifier

4.4 Pass Element and Voltage Divider

The pass element shown in Fig. 6a, is used to allow the excess input current to the load from the input source. It consists of two PMOS in series, where the M1 and M2 are biased with the output voltage of the error amplifier (OP_OUT) and V_{bias1}, respectively. Pass element controls the current delivered to the output capacitor. For a proper operation of the PMU, the pass element is designed in the strong inversion region [11]. To accommodate the deliverable current requirement ($\sim$ 1 mA), the dimension of the pass element is kept at $\frac{600\,\mu m}{180\,nm}$. The voltage divider or the resistive divider circuit shown in Fig. 6b at the output of the regulator is used to compare the output voltage V_{OUT} with the reference voltage V_{REF}. In order to divide the voltage equally across R1 and R2, values of R1 and R2 should be equal, ensuring that V_{REF} is half the value of the V_{OUT}. The resistors are diode connected MOSFETs. As shown in Fig. 7, reference voltage generates 0.475 V voltage at V_{IN} = 0.98 V using I_{PTAT} = 2.56 nA. It is also shown that the proposed PMU regulates V_{OUT} = 0.99 V, for V_{IN} = 1.76 V in no load condition. The variation in V_{REF} when V_{IN} changes is shown in Fig. 7, where a 30 mV slope is observed at V_{REF} when V_{IN} changes by 780 mV (from 0.98 V to 1.76 V).

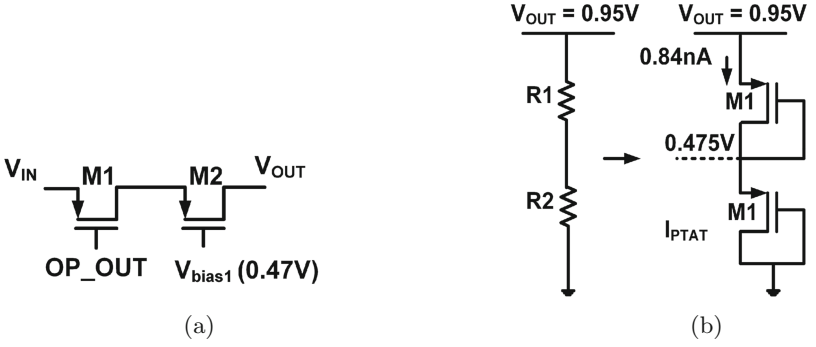


Fig. 6. (a) Pass Element for the Error Amplifier (b) Voltage Divider

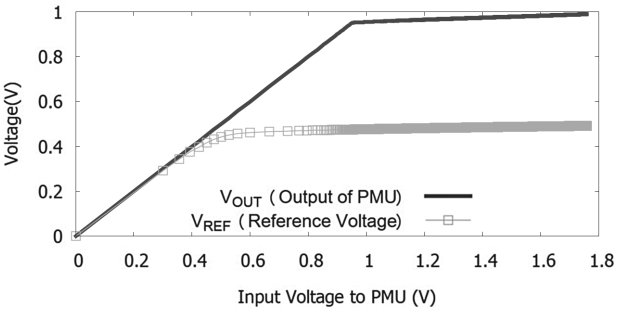


Fig. 7. Reference and Output Voltage of the PMU

4.5 Voltage Monitor

As shown in Fig. 8a, the voltage monitor [4] consists of two comparators and a DFF (D flip-flop) with an active low reset. The output voltage is regulated with DFF providing the Start/Stop signal for enabling or disabling the PMOS switch P1. It starts to generate the start signal at 0.76 V (= 0.8×0.95 V) and the stop signal at 0.57 V (= 0.6 × 0.95 V) as shown in Fig. 8b. The upper and lower threshold voltages for voltage monitor are fixed at $0.8V_{OUT}$ (∼ 0.8 V) and $0.6V_{OUT}$ (∼0.6 V). The values can be altered depending on the application. As soon as the regulator output voltage reaches the upper threshold voltage 0.8 V, voltage monitor connects the load (say an WSN) to the V_{OUT} via the switch P1. It disconnects the load resistor R_L from the output of the regulator as soon as the regulator output voltage decreases below the lower threshold voltage of 0.6 V. This ensures that sufficient energy is available for the WSN for reliable operation.

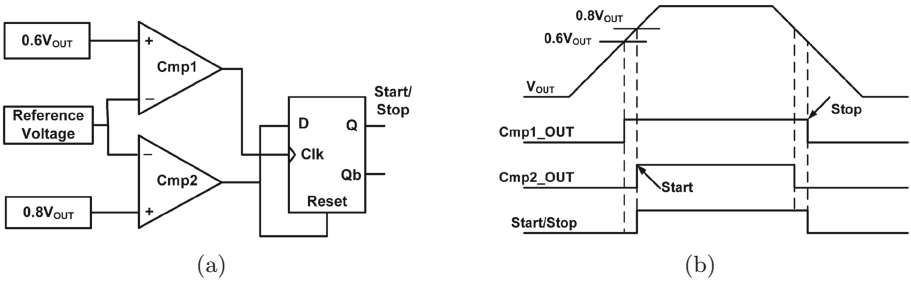


Fig. 8. Voltage Monitor (a) Block Diagram of Voltage Monitor (b) Ideal Response of Voltage Monitor

As can be seen in Fig. 8a, the output of first comparator Cmp1, is driven by lower threshold voltage and is connected to the clock terminal of DFF. The

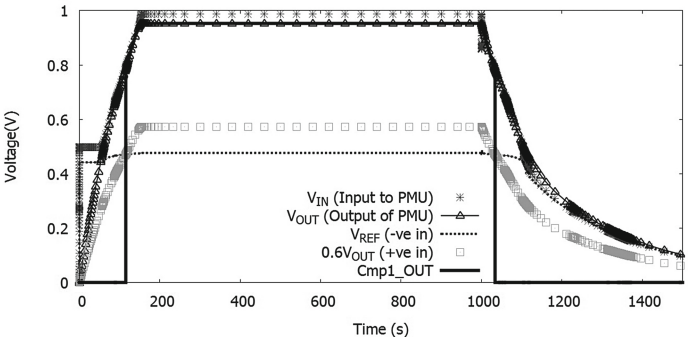


Fig. 9. Comparator output

output of second comparator Cmp2, is driven by upper threshold voltage, and is connected to the D input and the active low reset input. The ideal response of the voltage monitor is shown in Fig. 8b. During the operation of the voltage monitor, output of Cmp1 goes to logic high, when the regulator output voltage goes higher than 0.8 V (Start enabled). The output of Cmp2 will be logic low when the regulator output voltage becomes less than 0.6 V (Start disabled or Stop enabled). Approximately, 22 nA of current is consumed by the voltage monitor circuit. Out of which, 11 nA is consumed in each comparator and 10.16 pA is consumed in the DFF.

The transient behavior of the Cmp1 is shown in Fig. 9. As can be seen, when the positive terminal of the Cmp1, is at a higher voltage than 0.475 V (V_{REF}), the output Cmp1_OUT is at logic high.

5 Simulation Results and Discussion

The schematic simulations were carried out for different sub-blocks of the PMU, using 0.18 µm CMOS physical models. The output capacitor is chosen as 10 µF, a sufficient value for ULP WSN applications.

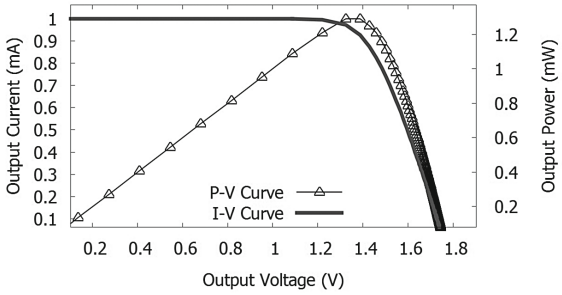


Fig. 10. I-V, P-V curves of the two series connected solar cells

In the simulation, input voltage for the PMU is generated by two series connected solar cells [12]. The I-V and P-V characteristics of the solar cells are shown in Fig. 10, where the solar cells equivalent model is characterized by short circuit current $I_{SC} = 1\,mA$ and the open circuit voltage $V_{OC} = 1.76\,V$. These solar cells can deliver upto 1.29 mW of maximum power to the PMU.

Two different conditions: one for low and the other for high input power are considered and discussed in the following sub-section. It is done to show the lower and higher boundaries of the PMU operation.

5.1 Analysis for Lower Value of Input Power

Various voltages are used for comparison in the voltage monitor is shown in Fig. 11. With $I_{Solar} = 70$ nA, $V_{IN} = 0.98$ V and the $V_{OUT} = 0.95$ V is observed. Therefore, $0.8V_{OUT}$ is equivalent to 0.76 V and $0.6V_{OUT}$ is equivalent to 0.57 V, is fed to the comparator block with that Start and Stop signals enabled correctly. We observed that out of the total current passing through the circuit, 32 nA current is delivered to the R_L and the rest 38 nA is consumed by the PMU. The complete transient response of the voltage monitor is shown in Fig. 12.

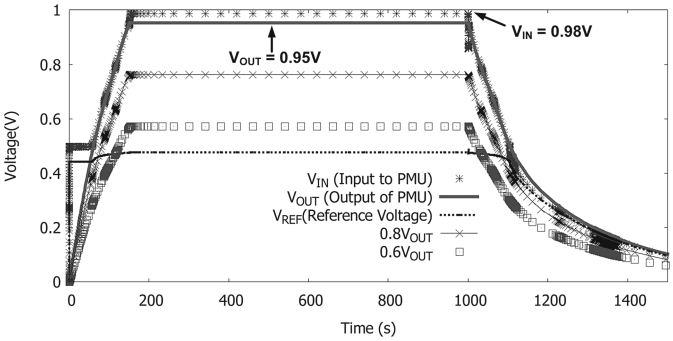


Fig. 11. Voltages used for comparison at lower input current

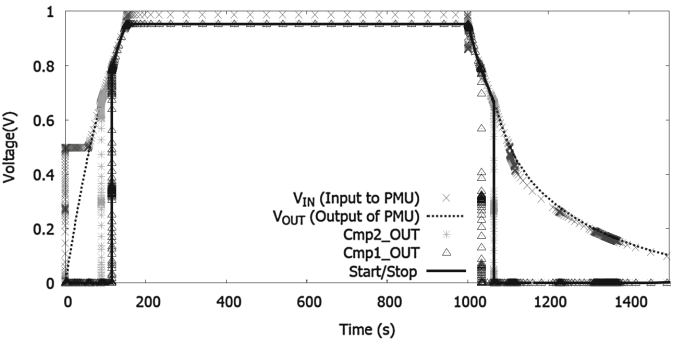


Fig. 12. Response of voltage monitor block

5.2 Analysis for Higher Value of Input Power

For a higher current, the simulation is carried out and is shown in Fig. 13. Input voltage $V_{IN} = 1.33\,\text{V}$ and $V_{OUT} = 0.968\,\text{V}$ are obtained at the input current, $I_{Solar} \sim 1\,\text{mA}$. Out of which 42 nA is consumed by the PMU the rest is deliver to R_L. Figure 14 presents the maximum linear regulator efficiency and regulator output voltage variation with the load current. As can be seen, the proposed PMU has a maximum efficiency of 72.3%. The PMU can also work with the higher load currents to a maximum of 1 mA. The output voltage is seen to be slightly decreased at a higher load current as shown in Fig. 14.

The current and power consumption of individual block of the PMU for both input voltages at 0.98 V and 1.33 V are shown in Table 2. The proposed PMU consumes 36 nW and 56 nW at $V_{IN} = 0.98\,\text{V}$ and $V_{IN} = 1.33\,\text{V}$, respectively. Furthermore, Table 3 compares the proposed PMU with the current work discussed in literature. From the Table 3, it can be concluded that proposed PMU has comparable power consumption and efficiency with respect to the mentioned work [4,5,7,13].

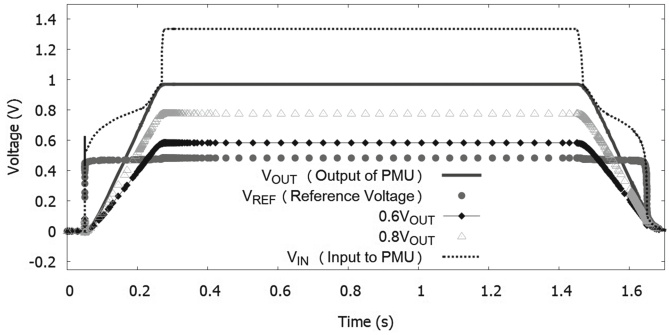


Fig. 13. Voltages used for comparison at higher input current

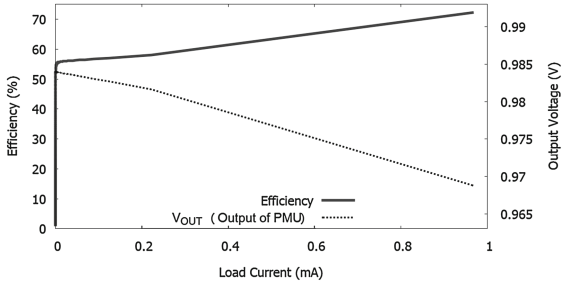


Fig. 14. Load analysis and PMU efficiency

Table 2. Power and Current consumption

Block	Sub-block	Current (A) (@ 0.98 V)	Power (W) (@ 0.98 V)	Current (A) (@ 1.33 V)	Power (W) (@ 1.33 V)
Regulator	Error amplifier	11.8n	11.2n	14.7n	20n
	Reference voltage	2.56n	2.43n	2.9n	4n
	Voltage divider	0.84n	0.8n	0.97n	1.3n
	Pass element	1.5p	1.43p	2p	2.7p
Voltage	Two comparators	21.8n	20.7n	22.15n	29.5n
Monitor	DFF	10.16p	9.65p	10.32p	13.7p
@PMU	-	38n*	36n	42n*	56n

* 1 nA current is consumed by insulation resistor kept in parallel with load capacitor to reduce leakage current through capacitor. Hence total current consumption and power consumption of the proposed PMU becomes 38 nA and 36 nW @0.98 V, and 42 nA and 56 nW @1.33 V, respectively.

Table 3. Performance comparison to reference works

Parameter	Proposed work	[4]	[5]	[7]	[13]*
Process	0.18 µm	0.18 µm	0.13 µm	0.18 µm	65 nm
Output voltage regulation (V)	0.95	1.8	1.4	1.0	-
Load current (mA)	1.0	25	0.005	0.6–1.1	-
Max efficiency (%)	72.3	-	58	70	-
Power dissipation (nW)	36	655	1400	-	50

* [13] is for Voltage Monitor Block only.

6 Conclusion

The proposed work presents the design of an ULP capacitive solar PMU. The proposed PMU is focused mainly on low power circuit blocks working at subthreshold voltages. Hence, all blocks of the PMU, except the pass element are designed in subthreshold region. At the input voltage of 0.98 V, the PMU regulates the output voltage to 0.95 V with 36nW of power consumption. For the input voltage of 1.33 V, it regulates the output voltage to 0.968 V with 56 nW power consumption and a maximum efficiency of 72.3%. The minimum voltage at which the PMU starts to operate is at 0.55 V and regulating the output at 0.98 V. Lower power consumption and better efficiency makes the PMU viable for various applications where low voltage, low power operations are required.

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