NIRMA UNIVERSITY

Institute of Technology

B. Tech Computer Science and Engineering

Semester IV

L	T	P	C
3	1	0	4

Course Code	**2CS401**
Course Title	**Computer Architecture**

Course Learning Outcomes (CLO):

At the end of the course, students will be able to –

1. outline and describe the basics of various architectural units of the Computer System
2. apply the knowledge of combinational and sequential logical circuits to mimic a simple computer architecture
3. design various architectural units of a basic computer system

Syllabus **Teaching hours:**

Unit I **10**

Register Transfer and Micro operations: Introduction to computer architecture, register transfer language -register transfer, bus and memory transfer, arithmetic micro operations, logic micro operations, shift micro operations and arithmetic logic shift unit. basic computer organization and design:instruction codes, computer registers, computer instructions, timing and control, instruction cycle, memory reference instructions, input-output and interrupt, complete computer description.

Unit II **10**

Micro Programmed Control: Control memory, address sequencing, micro program example, design of control unit. computer arithmetic: binary arithmetic's, add, subtract, multiply and divide, algorithms, and implementations carry look ahead and fast adders

Unit III 7

Central Processing Unit: Introduction, general register organization, stack organization, instruction formats, addressing modes, data transfer and manipulation, program control, reduced instruction set computer (RISC). Complex Instruction Set Computer (CISC), comparison of RISC and CISC parallel processing

Unit IV 6

Pipelining, Arithmetic pipelining, instruction pipelining, RISC pipeline, vector processing, Array processors

Unit V 6

Memory Organization: Memory hierarchy, main memory, auxiliary memory, flash memory, associative memory, cache memory, virtual memory

Unit VI 6

Input Output Organization: Peripheral devices, input output interface, serial communication, asynchronous data transfer, modes of transfer, priority interrupt, Direct Memory Access (DMA), Input Output processor (IOP)

Self-Study:

The self-study contents will be declared at the commencement of semester. Around 10% of the questions will be asked from self-study contents.

Tutorial Work:

Tutorial work will be based on above syllabus with minimum 10 tutorials to be incorporated.

Suggested Readings^:

1. Mano M, Computer System Architecture. Pearson Education
2. Stallings W, Computer Organization \& Architecture. Pearson Education
3. Hall D, Microprocessors and Interfacing 2E. McGraw-Hill Education (India) Pvt Limited
4. Hamacher C, Vranesic Z &Zaky S, Computer Organization. McGraw-Hill publishers
5. Balasubramanian D Comp Install And Servicing. McGraw-Hill Education (India) Pvt Limited

L = Lecture, T = Tutorial, P = Practical, C = Credit ^ this is not an exhaustive list