NIRMA UNIVERSITY

Institute:	Institute of Technology
Name of Programme:	BTech (CSE)
Course Code:	3CS517ME24
Course Title:	VLSI Programming
Course Type:	Department Elective-II
Year of Introduction:	2024-25

L	T	Practical Component				C
		LPW	PW	W	S	
3	0	2	-	-	-	4

Course Learning Outcomes (CLO):

At the end of the course, the students will be able to –

1. identify the various VLSI design styles, approaches, and IC fabrication design proce: (BL3)
2. analyse the CMOS-based circuit design (BL4)
3. design the various digital VLSI circuits (BL6)
4. develop the verification and testing of the VLSI circuit. (BL6)

Unit	Contents	Teaching Hours (Total 45)
Unit-I	**Fundamentals of VLSI:** Introduction of VLSI, Historical perspective, Objective and organization, Overview of VLSI Design Methodologies, VLSI design flow, Design Hierarchy, Concept of Regularity, Modularity and Locality, VLSI design Styles, Design Quality, Packaging Technology, CAD Technology	10
Unit-II	**MOSFET Basics:** Basics, V-I Characteristics, MOSFET scaling, Small-geometry effects, MOSFET capacitances, Switching in MOS, Challenges with MOS, MOS Alternate Technologies, Low Power Technology	10
Unit-III	**VLSI Design fundamentals:** Combinational and sequential MOS logic circuit designs	10
Unit-IV	**VLSI Verification:** Need for verification, Test bench, verification language, simulation tool, functional and code coverage.	10
Unit-V	**VLSI Testing:** Need of testing, roles of testing, fault methods, Introduction to High-level synthesis.	05

Self-Study:

The self-study contents will be declared at the commencement of the semester. Around 10% of the questions will be asked from self-study contents

Suggested Readings/ References:

1. Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis & Design, McGraw Hill
2. M. Bushnell, Vishwani Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Springer
3. Samir Palnitkar, Verilog HDL, SunSoft Press

Suggested List of Experiments:

Sr. No.	Title	Hours
1	Introduction of Hardware descriptor language (HDL) simulator.	04
2	Realization of Logic Gates using Verilog HDL	02
3	To design a half adder and a full adder using Verilog HDL	02
4	To design a 4X1 multiplexer using Verilog HDL	04
5	To design a 4-bit parallel adder using Verilog HDL	02
6	Write Verilog code for binary to gray code converter	02
7	To design a Decoder using Verilog HDL.	04
8	To design various Flipflops using Verilog HDL	02
9	To design and verify Logic Gates using Test Bench using Verilog HDL	04
10	To design and verify 4X1 multiplexer using Test Bench using Verilog HDL	02