NIRMA UNIVERSITY

Institute:	Institute of Technology, School of Technology
Name of Programme:	MTech CSE
Course Code:	6CS278ME25
Course Title:	Digital System Design
Course Type:	Department Elective-I
Year of Introduction:	2025-26

L	T	Practical Component				C
		LPW	PW	W	S	
3	0	2	-	-	-	4

Course Learning Outcomes (CLO):
At the end of the course, the students will be able to –

1. make use of the concepts of number system for representing numbers in different bases and performing arithmetic operations in various number systems (BL3)
2. apply the concepts of digital logic to develop a system using RTL (BL3)
3. simplify the Boolean logic using various techniques for sequential as well as combinational circuits (BL4)
4. design the digital system using behavioural modeling of Verilog and VLSI designing. (BL6)

Unit	Contents	Teaching Hours (Total 45)
Unit-I	**Introduction of the Digital System:** Number system, Complements, Number representation: BCD, floating point numbers	07
Unit-II	**Simplify Boolean Expressions:** Boolean algebra, application of Boolean algebra in minimization of Boolean expressions, Boolean minimization using K-map and Quine McCluskey method. Introduction to Verilog	07
Unit-III	**MSI Logic:** Multiplexer, encoder, decoder, Introduction to behavior modeling in Verilog	07
Unit-IV	**Arithmetic circuits:** Adder, subtractor, multiplier, comparator, Latches and flipflop (SR, JK, T, D), counters, Registers	07
Unit-V	**Sequential Circuits:** Finite state machine, state graphs and tables, Reduction of state table and state assignments. Arithmetic circuits using sequential design, Register transfer level (RTL) design, RTL design examples	07
Unit-VI	**VHDL/HDL Programming:** FPGA, VLSI design flow using HDL, introduction to behavior, logic, and physical synthesis.	10

Self-Study:
The self-study contents will be declared at the commencement of the semester. Around 10% of the questions will be asked from self-study content.

Suggested Readings/ References:

1. M. Morris Mano and Mechael D. Ciletti, Digital Design: with an introduction to Verilog HDL, Pearson
2. Michael D Ciletti, Advanced Digital Design with the Verilog HDL, Pearson
3. Roth and Kinney, Fundamentals of Logic Design, Cengage learning
4. Roth, John and Lee, Digital system design using Verilog, Cengage learning.

Suggested List of Experiments:

Sr. No.	Name of Experiments/Exercises	Hours
1	Perform the following combinational logic implementation using Logisim and Verilog HDL. i) Implement the simplified circuit for the given Boolean expression. ii) Implement a half-adder, full-adder, half-subtractor and full-subtractor circuits. iii) Implement the gate-level and behaviour modeling of various logic gates using Verilog - HDL iv) Implement the above circuit using Verilog and NAND gates. v) Design the combinational logic using a. multiplexer, b. decoder, c. ROMs and d. PLAs	08
2	Perform the following combinational logic implementation using Logisim and Verilog HDL. i) Implement the various flip-flops. ii) Design the sequential logic to implement a module – n synchronous counter. iii) Design the sequential logic to implement a module – n ripple counter. iv) Design a binary sequential adder using registers	08
3	Write a code in Verilog and HDL to implement the arithmetic circuits	06
4	Write a code in Verilog and HDL to implement the combinational logic	04
5	Write a code in Verilog and HDL to implement the sequential logic.	04