NIRMA UNIVERSITY

Institute:	Institute of Technology, School of Technology
Name of Programme:	MTech CSE, MTech CSE (Data Science)
Course Code:	6CS470ME25
Course Title:	System on Chip
Course Type:	Department Elective-III
Year of Introduction:	2025-26

L	T	Practical Component				C
		LPW	PW	W	S	
3	0	2	-	-	-	4

Course Learning Outcomes (CLO):

At the end of the course, the students will be able to:

1. interpret the System on Chip Design and its flow (BL2)
2. develop the System on Chip using Hardware Blocks/IPs (BL3)
3. analyse the performance of system on chip. (BL4)
4. design accelerator using Configurable Processors. (BL6)

Unit	Contents	Teaching Hours (Total 45)
Unit-I	**SOC Design**: Hardware System Structure, Software Structure, SOC Design Flow, The Impact of Semiconductor Economics, Major Issues in SOC Design	07
Unit-II	**SOC Accelerator Design:** Accelerating Processors for Traditional Software Tasks, System Design with Multiple Processors, Essentials of SOC Design Methodology	05
Unit-III	**System-Level Design of Complex SOCs:** Complex SOC System Architecture Opportunities, Major Decisions in Processor-Centric SOC Organization, Communication Design = Software Mode + Hardware Interconnect, Hardware Interconnect Mechanisms, Performance-Driven Communication Design, The SOC System Level Design Flow, Non-Processor Building Blocks in Complex SOC, Implications of Processor-Centric SOC Architecture	10
Unit-IV	**Configurable Processors:** A Software View, Processor Hardware/Software Cogeneration, The Process of Instruction Definition and Application Tuning, The Basics of Instruction Extension, The Programmer's Model, Processor Performance Factors, Example: Tuning a Large Task, Memory-System Tuning, Long Instruction Words	10
Unit-V	**Configurable Processors: A Hardware View:** Application Acceleration: A Common Problem, Introduction to Pipelines and Processors, Hardware Blocks to Processors, Moving from Hardwired Engines to Processors, Designing the Processor Interface, Novel Roles for Processors in Hardware Replacement, Processors, Hardware Implementation, and Verification Flow	07

Unit-VI	**Optimization in SOC Design:** Pipelining for Processor Performance, Inside Processor Pipeline Stalls, Optimizing Processors to Match Hardware, Multiple Processor Debug and Trace, Issues in Memory Systems.	06

Self-Study:

The self-study contents will be declared at the commencement of the semester. Around 10% of the questions will be asked from self-study content.

Suggested Readings/ References:

1. C. Rowen, Engineering the Complex SOC: Fast, Flexible Design with Configurable Processors, Prentice Hall
2. Daniel D. Gajski et al., Specification and Design of Embedded Systems, Prentice Hall
3. Henry Chang et al., Surviving the SoC Revolution, Kluwer Academic Publishers
4. Bassam Tabbara et al., Function/Architecture Optimization and Co-Design of Embedded Systems, Kluwer Academic Publishers
5. Michael Keating, Pierre Bricaud, Reuse Methodology Manual, Kluwer Academic Publishers
6. Frank Vahid, Tony Givargis, Embedded System Design, John Wiley & Sons, Inc
7. Steve Furber, ARM System-on-Chip Architecture, Addison Wesley.

Suggested List of Experiments:

Sr. No.	Name of Experiments/Exercises	Hours
1	System Modelling using UML	2
2	Event Driven Simulators: Gem5	2
3	Cycle Accurate Simulator: Gem5	2
4	Transaction Level Modelling: SystemC/Verilog/VHDL/simulators	2
5	Bus Functional Model (BFM): TLM Simulator	2
6	Instruction Set Architecture: Performance Measurement	2
7	Memory Hierarchy: Performance Measurement	2
8	Hardware Accelerator Design: Performance Measurement	2
9	Configurable Processor Architecture and Programming: Performance measurement	2
10	FPGA Design Tools: System Level Design	2
11	Mini Project: e.g. Digital Camera / ECG Monitoring.	10