NIRMA UNIVERSITY

Institute:	Institute of Technology
Name of Programme:	BTech CSE, Integrated BTech (CSE)-MBA
Course Code:	XXXX
Course Title:	Hardware Programming
Course Type:	Core
Year of Introduction:	2025-26

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Course Learning Outcomes (CLO):

At the end of the course, the student will be able to –

1. explain the basics of FPGA and its architecture (BL2)
2. demonstrate the basics of Hardware Description Language and VLSI design flow (BL3)
3. make use of behavioral modelling to design combinational and sequential circuits (BL3)
4. interpret the knowledge of logic circuits to perform the high-level synthesis. (BL5)

Unit	Contents	Teaching Hours (Total 30)
Unit-I	**Introduction:** Types of ASICs, ASIC cell libraries. VLSI design methodology, design flow, and challenges. Trends in HDL, Verilog/VHDL introduction and use in synthesis, Understanding the module and port. Timing and delay	08
Unit-II	**Modeling of combinational and sequential circuits using Verilog:** Designing multiplexer/data selector, comparator, latches, flip-flop, shift register, and counter using Verilog	07
Unit-III	**CMOS transistor theory:** Working of P-type and N-type transistors. Design of flip-flops using CMOS transistors. Levels of abstraction	05
Unit-IV	**Logic synthesis:** Code for optimal performance. Delay vs area, resource allocation. Two-level and multilevel gate-level optimization. Binary decision diagrams. Basic concepts of high-level synthesis: partitioning, scheduling, allocation, and binding. Technology mapping	06
Unit-V	**FPGA:** Latest FPGAs, FPGA CAD flow. Xilinx Spartan logic and routing.	04

Self-Study:

The self-study contents will be declared at the commencement of the semester. Around 10% of the questions will be asked from self-study content.

Suggested Readings/ References:

1. Samir Palnitkar, Verilog HDL, Pearson Education.
2. M. Morris Mano, Digital Design, PHI
3. Victor P. Nelson, Digital Logic Circuit Analysis and Design, Pearson Education.
4. Wayne Wolf, FPGA-based system design, Pearson Education
5. Pong P. Chu, FPGA Prototyping by Verilog Examples, Wiley.

Laboratory Work:
Laboratory work will be based on the above syllabus with a minimum of 10 experiments to be incorporated. The students in a suitable group size will design and perform one experiment as a part of Laboratory work.

Sr. No.	List of Experiments/Exercises	Hours
1	Introduction to lab hardware & software	02
2	Design and verify various logic gates using Verilog HDL.	06
3	Design an inverter and buffer using Verilog HDL	04
4	Design a decoder using Verilog HDL	04
5	4:1 Multiplexer in VHDL	04
6	Implement a 4:1 multiplexer in VHDL using: a. When-else statement b. Select statement c. Case statement	04
7	Multiplexer Design in Verilog a) Write a Verilog module to implement a 4-to-1 multiplexer using logic gates. b) Use this module along with additional logic to construct a 16-to-1 multiplexer.	04
8	Full Adder Implementation Write VHDL/Verilog code for a full adder. Design a full adder using half adders and implement it in VHDL using the structural style of modelling	04
9	Design a Flipflop using Verilog HDL	02
10	Write VHDL code for a D flip-flop using the dataflow style of modelling	06
11	8-Bit Shift Register in Verilog Design a Verilog module for an 8-bit shift registers with: a. Parallel load capability b. Synchronous clear c. Shift right functionality	04
12	4-Bit Ripple Carry Counter Design and implement a 4-bit ripple carry counter.	04
13	Write VHDL code for Mealy FSM using block statement.	04
14	Design Moore FSM and write VHDL code using behavioral style.	04
15	Write a Verilog module to check even parity for a serial data stream.	04