

## NIRMA UNIVERSITY

<b>Institute:</b>	<b>Institute of Technology</b>
<b>Name of Programme:</b>	<b>B. Tech. in Electrical Engineering</b>
<b>Semester:</b>	<b>III</b>
<b>Course Code:</b>	<b>2EE302</b>
<b>Course Title:</b>	<b>Digital Electronics</b>
<b>Course Type:</b>	<b>Core</b>
<b>Year of Introduction:</b>	<b>2023 – 24</b>

L	T	Practical component				C
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### Course Learning Outcomes (CLOs):

At the end of the course, the students will be able to –

1. Illustrate digital integrated circuits and characteristics (BL2)
2. make use of logic devices and design circuits based on the logic (BL4)
3. design and troubleshoot broad range of combinational and sequential circuits (BL4)
4. select and use Analog to Digital and Digital to Analog converters different applications (BL5)

### Syllabus:

**Teaching Hours: 30**

<b>Unit-1</b>	<b>Introduction</b>	<b>05</b>
	Number systems - Binary, hexadecimal, their conversion, representation of signed numbers and binary arithmetic in computers, weighted and non-weighted binary codes, BCD code, alphanumeric codes, Logic Gates - AND, OR, NOT, NAND, NOR X-OR and X-NOR, Boolean algebra, 7400 series (TTL) and 4000 Series (CMOS) integrated circuits, memory in computer system, memory types & terminology.	
<b>Unit-2</b>	<b>Karnaugh Map</b>	<b>03</b>
	Expression of Boolean function to SOP and POS forms, two, three and four variable Karnaugh map, merging & minimization of SOP & POS expressions, don't care combinations, five & six variable Karnaugh map.	
<b>Unit-3</b>	<b>Combinational Circuits</b>	<b>07</b>
	The half and full adder, the half & full subtractor, parallel binary adders, the look ahead carry adders, subtraction using parallel adders. BCD adders, code converters, parity bit generators/checkers, decoders, display devices, encoders, multiplexers, demultiplexers.	
<b>Unit-4</b>	<b>Sequential Circuits</b>	<b>07</b>
	S-R latch, gated latches, edge triggered S-R flip flop, J-K flip flop, D flip flop, T flip flop. flip flop operating characteristics, master – slave flip flops, application of flip flops, Buffer registers, controlled buffer register, 3-state buffer register, data transmission in shift register, serial in - serial out and parallel in - parallel out shift register, bi-directional shift register, application of shift register, asynchronous and synchronous counters, design and applications of counters.	
<b>Unit-5</b>	<b>Logic Families</b>	<b>03</b>
	Digital IC specification terminology, logic families: RTL, DTL, TTL, I <sup>2</sup> L, ECL & CMOS, TTL sub families, open collector gates, CMOS sub families, interfacing	

TTL to CMOS, interfacing ECL to other logics, applications.

**Unit-6 Analog to Digital and Digital to Analog Converters 05**

Digital to analog conversion, R-2R ladder type DAC, weighted resistor type DAC, the switched current source type DAC, counter type A/D converter, dual slope type A/D converter, successive approximation type A/D converter, applications.

**Self-Study:**

The self-study contents will be declared at the commencement of semester. Around 10% of the questions will be asked from self-study contents.

**Laboratory Work:**

This shall consist of at least 10 practical / simulations based on the above syllabus.

**Suggested Reading:**

1. Morris Mano, Textbook of Digital Logic and Computer Design, Pearson Education.
2. Bignell and Donovan, Textbook of Digital Electronics, Delmar (Thomson) Publication.
3. Charles Roth Jr., Larry Kinney, Raghunandan G. H., Analog and Digital Electronics, Cengage
4. A. Anandkumar, Textbook of Fundamentals of Digital Circuits, PHI Publication.
5. R.P. Jain, Textbook of Modern Digital Electronics, TMH Publications.
6. Anil K. Maini, Digital Electronics: Principles and Integrated Circuits, Wiley

**Suggested List of Experiments (not restricted to the following):  
(Only for Information)**

<b>Title of Experiment</b>	<b>Hrs.</b>
1. Realization and implementation of BCD parallel adder	2
2. Testing of parity generator (IC 74180) and realization of 8-bit parity checker	2
3. Analyze 8-to-1 line multiplexer and realize a Boolean function	4
4. Analyze digital demultiplexer (IC 74138) and realize full adder	4
5. Design BCD to seven-segment decoder	2
6. Verify truth tables of RS, JK, D and T flip-flops	2
7. Design and realization of binary ripple counter	2
8. Design and realization of modulo 10 binary synchronous counter using J-K flip-flops	2
9. Realization of binary shift register	2
10. Realization of digital to analog converter	2

L = Lecture, T = Tutorial, P = Practical, C = Credit

w.e.f. academic year 2023 - 24 and onwards