# NIRMA UNIVERSITY
# SCHOOL OF TECHNOLOGY, INSTITUTE OF TECHNOLOGY
# M. Tech. in Electronics & Communication Engineering (VLSI Design)
# M.Tech Semester - I

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| **Course Code** | **6EC105** |
| **Course Title** | **VLSI Physical Design** |

**Course Learning Outcomes (CLOs)**:

At the end of the course, students will be able to -

1. Apply the concepts of graph theory
2. Comprehend and apply various algorithms to circuit partitioning Floor planning, Placement and Routing
3. Implement the VLSI physical design using CAD tools

**Syllabus:** **Teaching Hours: 45**

**UNIT I:** **05**
Introduction to Graph Theory, Dependency/ Constraint graphs; Steiner Tree; Cliques, Clustering and Spanning Tree

**UNIT II:** **10**
Circuit Level Petitioning, cost function and constrains, Algorithm for Circuit partitioning

**UNIT III:** **15**
Floorplanning and Pin Allocation, problem definition and cost functions

**UNIT IV:** **08**
Placement and Routing, Algorithms, cost function and constrains, Area routing, Design Rule Check issue

**UNIT V:** **02**
Basic Concepts in Clock Networks, Modern Clock Tree Synthesis

**UNIT VI:** **05**
Timing closure, Timing Analysis and Performance constrains, Timing driven placement and routing, Physical synthesis

## Self Study:
The self-study contents will be declared at the commencement of semester. Around 10% of the questions will be asked from self-study contents

## Laboratory work:
Laboratory work will be based on above syllabus with minimum 10 experiments to be incorporated.

## Suggested Readings:

1. Sadiq M Sait,Habib Youssef ,VLSI Physical Design Automation: Theory and Practice Publication: World Scientific
2. Andrew B Kahng, Jens Lienig VLSI Physical Design: From Graph partitioning to Timing Closure, Publication: Springer
3. Sung Kyu Lim , Practical Problems in VLSI Physical Design Automation, 2008 edition, Springer