VLSI Chip Design using Cadence

Hands on Workshop

Coordinators:
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April 28 – 29, 2023

TARGET AUDIENCE
✓ Final and Pre-Final year B. E./B. Tech Students
✓ Students of M. E./M. Tech and Ph. D.
✓ Faculty Members of Engineering Colleges
✓ Industry Personnel

OBJECTIVES OF THE PROGRAM

Modern era is driven by integrated electronics. VLSI design is considered as the most important aspect of the modern electronics. The objective of the programme is to impart the VLSI design knowledge using the state-of-the-art EDA tools. The digital, analog and RF VLSI design are the major highlights of the programme. The workshop is dedicated to the hands-on experimental work for the simulations and layout designs of the digital, analog and RF VLSI circuits. Looking to the trend of VLSI Design, this workshop is intended for those who are faculty of Technical Institutes teaching or doing research in the areas of VLSI Design and Engineers from industry who want to explore EDA design flow. It can also be attended by research scholars and PG students who would like to be specialized in VLSI.

COURSE REGISTRATION
✓ Rs. 300/- for Students (+18% GST)
✓ Rs. 500/- for Other than Students (+18% GST)

Course materials will be provided to all the participants. Participants. Registration charges are non-refundable. Participants will be provided with chargeable boarding facilities on request on first come first serve basis. Participants will have to make their own arrangements for travelling.

After the payment, fill the online registration form by scanning the QR code. Upload the photo of proof of payment in the form.

Fees can be paid by Online mode only. The payment can be done by IMPS/NEFT/RTGS to the following account:

Bank	:	The Kalupur Com. Co. Op. Bank Ltd
Account	:	Institute of Technology, Under Nirma University
Account No	:	09720180111
IFSC Code	:	KCCB0NRM097

OUTLINE OF CONTENT
✓ Basics of digital, analog and RF VLSI design.
✓ Testing and verification of VLSI circuits
✓ Overview of EDA design flow.
✓ Digital, Analog and RF circuit simulations.
✓ Circuit layout generation
✓ Post layout simulations flow
✓ Process variations, Corner analysis and Monte Carlo simulations using EDA tools.

For More Information and Registration:

https://sites.google.com/nirmauni.ac.in/vdvc/home

Organized by
Department of Electronics and Communication Engineering
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