Institute:	Institute of Technology
Name of Programme:	B.Tech. Electronics & Communication Engineering
Course Code:	2EC201
Course Title:	Digital Logic Design
Course Type:	(■ Core/ ☐ Value Added Course/☐ Departmental Elective/ ☐ Institute Elective/ ☐ University Elective/ (☐ Open Elective Any other)
Year of Introduction:	2023-24

Credit Scheme

L	T	Practical component				C
		LPW	PW	W	S	
2	-	2	-	-	-	3

Course Learning Outcomes (CLOs):

At the end of the course, students will be able to –

1. optimise the Boolean equations using k-map and tabulation method. BL 2
2. develop the combinational digital circuits for the given specification. BL 4
3. design and implement sequential digital circuits. BL 5
4. construct digital systems using Verilog HDL. BL 5

Unit No.	Syllabus	Teaching hours
I	**Boolean Expression Optimisation** Binary Arithmetic, Basic Gates, Design using Universal Gates, K-map and minimisation of POS and SOP expressions, Don't care conditions, N's Complement Arithmetic	09
II	**Combinational Circuits** Basics of Combinational logic design, Adder and Subtractor, Parallel adders, BCD adder, Code converters, Comparators, Encoder, Decoder, multiplexer, demultiplex, application, concept of PAL, PLA	08
III	**Sequential Circuits** Introduction to sequential circuits, S-R Flip-flop, D Flip-flop and JK Flip-flop, T Flip-flop and Race around conditions, Edge –Triggered Flip-flops, Master-slave Flip-flop. Design of Synchronous and Asynchronous Counters, Shift Registers	08
IV	**Logic Families** Digital IC specification terminology, TTL, CMOS	02
V	**Hardware Description Languages (Verilog)** Fundamentals of Verilog, Overview of digital design with Verilog HDL, Gate Level Modelling, Dataflow Modelling, Behavioural Modelling	03

Self Study:

The self-study contents will be declared at the commencement of semester. Around 10% of the questions will be asked from self-study contents.

Laboratory Work:

Laboratory work will be based on above syllabus with minimum 10 experiments to be incorporated.

List of Experiments:

Sr. No.	Title of the experiment	Hours
1.	Implementation of Boolean function using logic gates.	02
2.	Design and implementation of half and full adders and subtractors.	02
3.	Design and implementation of multiplexer and Boolean function using multiplexer.	02
4.	Design and implementation of an encoder and decoder.	04
5.	Design and implementation of Flip Flops.	02
6.	Design of Shift Register and variants.	02
7.	Design and implementation of Counters.	02
8.	Digital hardware design flow with Verilog HDL.	02
9.	Dataflow style of modelling using Verilog HDL.	02
10.	Structural style of modelling using Verilog HDL.	02
11.	Behavioural style of modelling using Verilog HDL.	02
12.	Design and implementation of magnitude comparator in Verilog HDL.	02
13.	Design and implementation of flipflops in Verilog HDL.	02
14.	Design and implementation of Counter in Verilog HDL.	02
15.	Design and implementation of Arithmetic and Logic unit in Verilog HDL.	02

Suggested Readings:

1. M. Morris Mano, Digital logic and computer Design, PHI.
2. A. Anand Kumar, Fundamentals of Digital Circuits, PHI.
3. Thomas A. Demassa and Zack Ciccone, Digital Integrated Circuits, Wiley Publications.
4. Charles H. Roth, Jr. Lizy Kurian and John Byeong Kil Lee, Digital Systems Design using Verilog, Cengage Learning India, 2016.
5. Samir Palnitkar, Verilog® HDL: A Guide to Digital Design and Synthesis, Prentice Hall PTR.