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|---|---|
| **Institute:** | Institute of Technology |
| **Name of Programme:** | B.Tech. Electronics & Communication Engineering |
| **Course Code:** | 2EC202 |
| **Course Title:** | FPGA based System Design |
| **Course Type:** | (■ Core/ □ Value Added Course/□ Departmental Elective/ □ Institute Elective/ □University Elective/ □ ( Open Elective Any other) |
| **Year of Introduction:** | 2023-24 |

**Credit Scheme**

| L | T | Practical component | | | | C |
|---|---|---|---|---|---|---|
| | | LPW | PW | W | S | |
| 2 | - | 2 | - | - | - | 3 |

**Course Learning Outcomes (CLOs):**

At the end of the course, students will be able to –

1. implement combinational digital circuits. BL 3
2. develop synchronous and asynchronous digital circuits. BL 5
3. design and develop finite state machine based digital systems. BL 5
4. construct digital systems using Hardware Description Language on reconfigurable devices. BL 6

| Unit No. | Syllabus | Teaching hours |
|---|---|---|
| I | **Introduction to Digital Systems Design**<br>Overview of digital fundamentals, design with LSI and MSI Logics, Advanced Boolean algebra and logic optimisation, Hazards in combinational networks | **06** |
| II | **Synchronous Finite State Machines**<br>Design of synchronous sequential machines: Mealy and Moore machine, Counter design using sequential Machines, Multimode Counters, Reduction of state table and state assignment, Design of sequence detectors and code converters, Timing and Triggering consideration in a sequential machine, Clock skew. | **08** |
| III | **Asynchronous Finite State Machine**<br>Asynchronous sequential circuit analysis, primitive flow table, the concept of race, critical race and hazards, design issues like metastability, synchronisers, clock skew and timing considerations, Design of Asynchronous Machines. | **05** |
| IV | **Programmable Logic and Reconfigurable Device Architectures**<br>Architecture of ROM, PROM, PAL and PLA, System controller design using PROM, PAL and PLA, Classification of FPGA, Basic architecture of CPLD and FPGA | **06** |
| V | **HDL based System Design**<br>Digital Design with Verilog HDL, Data Types on Verilog, Arrays in Verilog, Tasks and Functions, FSM based Design using Verilog, RTL Description of Simple Machine and Design from RTL description, Test Bench, IP core-based designs | **05** |

**Self Study:**

The self-study contents will be declared at the commencement of semester. Around 10% of the questions will be asked from self-study contents.

**Laboratory Work:**
Laboratory work will be based on above syllabus with minimum 10 experiments to be incorporated.

**List of Experiments:**

| Sr. No. | Title of the experiment | Hours |
|---|---|---|
| 1 | Switch level modelling using Verilog HDL. | 02 |
| 2 | Digital hardware design flow and modelling with Verilog HDL. | 02 |
| 3 | Design and implementation of Arithmetic circuits on FPGA. | 02 |
| 4 | Implement, Synthesise and Simulate flip flops circuits. | 02 |
| 5 | Design and implementation based on Mealy FSM on FPGA. | 02 |
| 6 | Design and implementation based on Moore FSM on FPGA. | 02 |
| 7 | Design, Implement, simulate and synthesis the following using Verilog | 02 |
| 8 | ALU : 8 bit with ADD, SUB, AND, OR, NOT, XOR, SHL, SHR, ROL, ROR, CMP features and flags : C, AC, Z, S, P | 04 |
| 9 | Design, Implement, simulate and synthesise "4-bit shift register with parallel loading, parallel output, serial in-out capability" using VERILOG. | 02 |
| 10 | Design and Implement Mealy and Moore based machine using state diagram entry. | 02 |
| 11 | Design and implement 1024 X 8 ROM on FPGA. | 02 |
| 12 | Design and implementation of RAM on FPGA. | 02 |
| 13 | Design and implementation of FIFO on FPGA. | 06 |
| 14 | Design and Implement Generic Up/Down counter using Block Diagram / Schematic file in Quartus-II | 02 |
| 15 | Design, Implement, simulate and synthesis 8-bit signed multiplier using IP CORE Generator System | 02 |

**Suggested Readings**:


1. C.V.S. Rao, Switching Theory & Logic Design, Pearson Education
2. Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Pearson Education
3. Charles H. Roth Jr, Lizy Kurian John - Principles of Digital System Design Using Verilog, Cengage Learning
4. William I. Fletcher, An Engineering Approach to Digital Design, Prentice Hall of India
5. Chan and Mourad, Digital Design using Field Programmable Gate Arrays, Prentice Hall of India