NIRMA UNIVERSITY

Institute:	Institute of Technology
Name of Programme:	B.Tech. Electronics & Communication Engineering
Course Code:	3EC601CC24
Course Title:	VLSI Design
Course Type:	Core
Year of Introduction:	2024-25

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Course Learning Outcomes (CLOs):

At the end of the course, students will be able to

1. analyse the digital VLSI circuits working with Resistive load, NMOS, PMOS and CMOS load conditions under linear and saturation region. BL-3
2. evaluate digital VLSI circuits for speed, area, power, cost and output voltage requirements. BL-4
3. design combinational, sequential and dynamic logic circuits using CMOS for given specifications. BL-5
4. simulate and optimise digital VLSI circuits and layouts of the same using EDA tool. BL-5

Unit No.	Contents	Teaching hours (Total 45)
I	**Introduction of VLSI:** Historical perspective, objective and organisation, overview of VLSI design methodologies, VLSI design flow, design hierarchy, concept of regularity, modularity and locality, VLSI design styles, design quality, packaging technology, CAD technology.	02
II	**MOS Basics Scaling and Effects of Scaling on MOS:** MOSFET basics, V-I characteristics, MOSFET scaling, small-geometry effects, MOSFET capacitances	07
III	**MOS inverter Static characteristics:** Introduction, resistive load inverter, inverter with n-type MOSFET load (enhancement & depletion type MOSFET load), CMOS Inverter.	08
IV	**MOS inverters Switching characteristics and Interconnect Effects:** introduction, delay-time definitions, calculation of delay times, inverter design with delay constraints, estimation of interconnect parasitic, calculation of interconnect delay, switching power dissipation of CMOS inverters.	07
V	**MOS based Logic circuits:** Introduction, MOS logic circuits with depletion NMOS Loads, CMOS logic circuits, complex logic circuits, CMOS Transmission Gates (TGs). behavior of bistable elements, SR latch circuit, clocked latch & flip-flop circuit, CMOS D-latch & Edge-triggered flip-flop.	11
VI	**Dynamic Logic Circuits:** Introduction, basic principles of pass transistor circuits, synchronous dynamic circuit techniques, CMOS dynamic circuit techniques.	07
VII	**Advances in VLSI Design:** Problems with MOS, MOS alternate devices	03

Self-Study:

The self-study contents will be declared at the commencement of the semester. Around 10% of the questions will be asked from self-study content.

Laboratory Work:
Laboratory work will be based on the above syllabus with a minimum of 10 experiments to be incorporated.

Suggest List of Experiments (not restricted to the following):
(Only for information)

Sr. No.	Title of the experiment	Hours
1.	To get acquainted with EDA tool for layout design. Experiment with design rule checks for layout design.	02
2.	To design resistive load inverter and prepare the layout of the same. To find values of voltages associated with VTC curve. Simulate the inverter for finding the transient response, propagation delays, and rise and fall times.	02
3.	To design inverter with active load and prepare the layout of the same. Find values of voltages associated with VTC curve. Simulate the inverter for finding the transient response, propagation delays, and rise and fall times.	02
4.	To design CMOS inverter and prepare the layout of the same. Find values of voltages associated with VTC curve. Simulate the inverter for finding the transient response, propagation delays, and rise and fall times.	02
5.	To simulate the output and transfer characteristics of MOS transistors for finding out technology parameters using LTSpice.	02
6.	To design CMOS NAND gate and prepare the layout t of the same and find equivalent W/L ratio for series and parallel combinations of MOS transistors also simulate the gates for finding the transient response, propagation delays, and rise and fall times.	02
7.	To design CMOS NOR gates and prepare the layout t of the same and find equivalent W/L ratio for series and parallel combinations of MOS transistors also simulate the gates for finding the transient response, propagation delays, and rise and fall times.	02
8.	To design and implement CMOS based ring oscillator for given specifications. Prepare the layout for the same and compare the simulated results with the theoretical results.	02
9.	To Prepare the layout for clocked SR Latch. Simulate the latch to find out transient response, propagation delays, and rise and fall times.	02
10.	To Prepare the layout for clocked D Latch. Simulate the latch to find out transient response, propagation delays, and rise and fall times.	02
11.	To Prepare the layout of CMOS transmission gate. Simulate the same for the value of resistance with change in voltage across it. Verify the wired OR logic of transmission gate. Apply the transmission gate to prepare a 2x1 MUX.	02
12.	Design D flip flop using CMOS Transmission gate.	02
13.	To Prepare the layout for two stage combinational circuit using Pre-Charge Evaluate logic.	02
14.	To Prepare the layout for two stage combinational circuit using domino logic.	02
15.	To implement pipelining in dynamic CMOS logic circuits.	02

Suggested Readings:

1. Sung Mo kang, Yusuf Leblebici, CMOS Digital Integrated circuits – Analysis and Design, Tata McGraw-Hill.
2. Pucknell & Eshraghian, Basic VLSI Design, PHI
3. Amar Mukerji, Introduction to nMOS and CMOS VLSI System Design, Prentice Hall
4. Neil H. E. Weste, David Money Harris, CMOS VLSI Design - A Circuits and Systems Perspective, Addison – Wesley.