NIRMA UNIVERSITY

Institute:	Institute of Technology
Name of Programme:	MTech Semiconductor Technology
Course Code:	6EC101CC22
Course Title:	Digital VLSI Design
Course Type:	Core
Year of Introduction:	2024-25

L	T	Practical component				C
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Course Learning Outcomes (CLOs)

At the end of the course, students will be able to

1. evaluate characteristics of CMOS inverter (BL4)
2. analyse and design digital circuits using CMOS constrained by the design metrics (BL5)
3. optimize the layout of CMOS based digital circuits (BL5)
4. use commercial CAD tools for design and optimization. (BL6)

	Contents	Teaching hours (Total 45)
Unit I	**Introduction to VLSI** Introduction to VLSI design flow, VLSI design Methodologies, Design Hierarchy, Concept of Regularity, Modularity and Locality, VLSI design Styles.	**03**
Unit II	**Static Characteristics of MOS Inverter** Introduction, Voltage Transfer Characteristics (VTC) of Inverter, Significance of Noise Margins, Resistive-Load Inverter, n-type MOS Load Inverter, CMOS Inverter	**10**
Unit III	**Combinational MOS Logic Circuits** NOR and NAND Gates with Depletion nMOS Loads, Transient Analysis, CMOS NOR2 and NAND2 Gates, AOI Implementation, Pseudo-nMOS Gates, Complementary Pass-Transistor Logic (CPL), CMOS Full Adder, CMOS Transmission Gate (Pass Transistor), Effective W/L Calculations, Layout, Euler's Path, Stick Diagram.	**10**
Unit IV	**Sequential MOS Logic Circuits** NOR and NAND based SR Latch Circuits, Clocked-based SR Latch, Clocked JK Latch, CMOS D-Latch and Edge-Triggered Flip-Flop.	**10**
Unit V	**Dynamic Logic Circuits** Introduction, Basic Principles of Pass Transistor Circuits, Synchronous Dynamic Circuit Techniques, CMOS Dynamic Circuit Techniques.	**07**
Unit VI	**CMOS Circuit Modeling using Tools and Technology** PSPICE Model, Switch Level Modeling using Verilog Hardware Description Language (HDL)	**05**

Self Study:
The self-study contents will be declared at the commencement of the semester. Around 10% of the questions will be asked from self-study content.

Laboratory Work:
Laboratory work will be based on the above syllabus with a minimum of 10 experiments to be incorporated.

Suggested Readings/References:

1. Sung Mo kang, Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis and Design, TATA McGraw-Hill.
2. Neil H. E. Weste, David Money Harris, CMOS VLSI Design A Circuits and Systems Perspective, Addison Wesly.
3. Jhon E. Ayers, Digital Integrated Circuits Analysis and Design, CRC Press

Details of Laboratory
Suggested List of Experiments

Sr. No.	Practical	No. of Hours
1.	To get acquainted with CAD tool for layout design. Understand the design rule checks for layout design.	02
2.	To design resistive load inverter and prepare the layout.	02
3.	To design inverter with active load and prepare the layout of the same.	02
4.	To design CMOS inverter and prepare the layout. Plot the VTC curve and analyse the parameters.	02
5.	To design CMOS-based 2-input NAND gate, prepare the layout and analyse the parameters.	02
6.	To design CMOS-based 2-input NOR gate, prepare the layout and analyse the parameters.	02
7.	To design complex function using CMOS logic, prepare the layout and find equivalent W/L ratio.	02
8.	To design D latch and prepare the layout.	02
9.	To Prepare the layout for clocked SR Latch.	02
10.	To implement Boolean function using CMOS transmission gate.	02
11.	Design combinational circuit using CMOS Transmission gate.	02
12.	Design D flip flop using CMOS Transmission gate.	02
13.	To develop SPICE code for combinational CMOS circuits.	02
14.	To design combinational CMOS circuit using switch level modeling	02
15.	To design sequential CMOS circuit using switch level modeling	02