

NIRMA UNIVERSITY

Institute:	Institute of Technology
Name of Programme:	MTech Semiconductor Technology
Course Code:	6EC167CC22
Course Title:	Memory Technology
Course Type:	Departmental Elective
Year of Introduction:	2024-25

L	T	Practical component				C
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Course Learning Outcomes (CLOs)

At the end of the course, students will be able to

1. comprehend the architecture of RAM and non-volatile memory (BL3)
2. apply reliability modelling and failure modes to memory design (BL4)
3. develop the memory cell using advanced technology (BL4)
4. design memory array. (BL5)

Contents

	Contents	Teaching hours (Total 45)
Unit I	Static Random Access Memory Technologies MOS RAM technologies, SRAMs, architecture, SRAM cell and peripheral, Circuit operation, SRAM Technologies, SOI Technology, advanced SRAM architectures and technologies, DRAM technology development, CMOS DRAMs cell, theory and advanced cell structures	10
Unit II	Embedded Memory Designs Nonvolatile memories, MOS ROMs, PROMs, EPROMs, One-Time Programmable EPROMs, EEPROM technology and architecture, Nonvolatile SRAM-Flash Memories, advanced Flash Memory architecture	10
Unit III	Failure Memory Directions Memory failure modes, reliability modelling, Prediction design for reliability, reliability test structures, reliability screening and qualification, radiation effects, radiation hardening, process and techniques, Radiation hardened memory characteristics, soft errors	10
Unit IV	Advanced Memory Designs Ferroelectric random-access memories (FRAMs), Gallium arsenide FRAMs, Analog memories, Magneto resistive RAMs, Experimental memory devices, Memory hybrids and MCMs (2D), Memory stacks and MCMs(3D), memory cards,	08

	high density memory packaging	
I.	Memory Testing RAM Fault Modelling, Memory Testing Algorithms, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Non-volatile Memory Modelling and Testing, IDDQ Fault Modelling and Testing-Application Specific Memory Testing	05
II.	Memory Packaging Memory Hybrids (2D & 3D), Memory Stacks, Memory Cards, High Density Memory Packaging	02

Self-Study:

The self-study contents will be declared at the commencement of Semester. Around 10% of the questions will be asked from self-study contents.

Suggested Readings/References:

1. Ashok K. Sharma, Advanced Semiconductor Memories: Architectures, Designs, and Applications, John Wiley
2. Ashok K. Sharma, Semiconductor Memories Technology, Testing and Reliability, IEEE Press
3. Kiyoo Itoh, VLSI Memory Chip Design, Springer International Edition
4. Santosh K. Kurinec, Krzysztof Iniewski, Nanoscale Semiconductor Memories: Technology and Applications, CRC Press