NIRMA UNIVERSITY

Institute:	Institute of Technology
Name of Programme:	MTech Semiconductor Technology
Course Code:	6EC303CC24
Course Title:	Semiconductor Process Technology
Course Type:	Core
Year of Introduction:	2024-25

L	T	Practical component				C
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Course Learning Outcomes (CLOs)

At the end of the course, students will be able to

1. use of fundamental principles of semiconductor device fabrication (BL3)
2. distinguish the various processes involved in semiconductor manufacturing (BL4)
3. perceive about the latest advancements and trends in the semiconductor industry (BL5)
4. develop skills in analysing and optimizing semiconductor process technologies (BL6)

	Contents	Teaching hours (Total 45)
Unit I	**Overview** Introduction and overview of micro and nano fabrication technology, invention of the transistor, emergence of Silicon Valley, Moore's Law **Crystal growth** (Czochralski, Float-Zone) and wafer engineering (slicing, polishing, and cleaning processes)	**09**
Unit II	**Clean room** Safety and contamination issues in a cleanroom, overview of cleanroom hazards, basic process flow structuring, wafer type selection and cleaning methods, additive fabrication processes	**06**
Unit III	**Materials Deposition Methods** Physical vapour deposition methods (thermal, molecular beam evaporation) and chemical vapour deposition methods (PE-CVD, MOCVD), sputtering (DC and RF), spin coating, spray pyrolysis, pulsed laser deposition (PLD), diffusion (mechanism and process) and ion implant techniques, oxidation techniques and kinetics, LOCOS techniques	**09**
Unit IV	**Etch and Cleaning** Materials used in cleaning, various cleaning methods, wet etch, dry etch, plasma etching, RIE etching, etch selectivity/selective etch	**06**
Unit V	**Photolithography** Optical lithography fundamentals- contact lithography, stepper/canner lithography, holographic lithography, DSW, e-beam lithography, ion beam lithography, lift off techniques, next generation technologies: Immersion lithography, phase shift mask, X-ray lithography	**10**

Unit VI **Planarization Techniques** **05**

Need for planarization, chemical mechanical polishing(CMP), metallization and interconnects: copper damascene process, metal interconnects, multi-level metallization schemes, process integration: NMOS, CMOS and Bipolar process

Self-Study:

The self-study contents will be declared at the commencement of the semester. Around 10% of the questions will be asked from self-study content.

Laboratory Work:

Laboratory work will be based on the above syllabus with a minimum of 10 experiments to be incorporated.

Suggested Readings/References:

1. James Plummer, M. Deal and P. Griffin, Silicon VLSI Technology, Prentice Hall.
2. Ayers J. E, Heteroepitaxy of Semiconductors Theory, Growth, and Characterization , CRC Press, Taylor & Francis.
3. Stephen A. Campbell, The Science and Engineering of Microelectronic Fabrication,
4. Oxford University Press.
5. Sze, S.M., Semiconductor Devices: Physics and Technology, John Wiley and Sons.

Details of Laboratory
Suggested List of Experiments

Sr. No.	Practical	No of Hours
1.	To learn the sputtering process for depositing metal films, such as aluminium or copper, on semiconductor/ glass substrates and to measure sheet resistance by four point probe method.	04
2.	To study the process of depositing thin films of materials such as silicon dioxide or silicon nitride using chemical vapor deposition techniques.	04
3.	To grow silicon oxide film on silicon wafer by CVD technique.	04
4.	To grow a silicon dioxide layer on a silicon substrate using dry and wet oxidation processes and to measure the oxide thickness.	04
5.	To measure the thickness of thin films, analyse surface and cross-sectional features using SEM, and perform crystallographic analysis using XRD.	04
6.	To deposit dielectric materials and characterize their properties using capacitance-voltage (C-V) measurements to extract dielectric constants.	04
7.	To understand and implement procedures for maintaining a cleanroom environment and measure particle contamination levels using particle counters.	04