NIRMA UNIVERSITY

Institute:	Institute of Technology
Name of Programme:	MTech Semiconductor Technology
Course Code:	6EC304CC24
Course Title:	Physical Design of CMOS Technology
Course Type:	Core
Year of Introduction:	2024-25

L	T	Practical component				C
		LPW	PW	W	S	
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Course Learning Outcomes (CLOs)

At the end of the course, students will be able to

1. study various phases of physical design for semiconductor technology (BL3)
2. use of algorithms to perform portioning, floorplanning, placement and routing (BL4)
3. apply the data structure and graph theory to physical design (BL5)
4. optimise the design by applying physical design algorithms through CAD tools. (BL6)

	Contents	Teaching hours (Total 45)
Unit I	**Graph Theory for Physical Design** Basic Terminology, Complexity Issues and NP-hardness Algorithms for NP-hard Problems, Graph Theory, Graph Algorithms for Physical Design.	**05**
Unit II	**Partitioning** Introduction and Optimization goals, Classification of Partitioning Algorithms, Kernighan-Lin Algorithm, Extensions of Kernighan-Lin Algorithm, Fiduccia-Mattheyses Algorithm, Simulated Annealing and Evolution, Multilevel Partitioning Circuit level petitioning, Cost Function and Constraints.	**08**
Unit III	**Floorplanning** Classification of Floorplanning Algorithms, Constraint Based Floorplanning, Chip Planning, Pin Assignment, Problem Formulation, Pin Assignment Algorithms.	**08**
Unit IV	**Placement** Classification of Placement Algorithms, Simulation Based Placement Algorithms, Cluster Growth, Performance Driven Algorithms.	**08**
Unit V	**Global and Detailed Routing** Classification of Routing Algorithms, Single-Layer Routing Algorithms, Maze Routing Algorithms, Shortest Path Based Algorithm, Clock and Power Routing.	**10**
Unit VI	**Clock and Timing:** Basic concepts of Clock Networks, Clock Tree Synthesis, Timing Closure, Timing Analysis and Performance Constraints, Timing Driven Placement and Routing, Physical Synthesis.	**06**

Self -Study:
The self-study contents will be declared at the commencement of semester. Around 10% of the questions will be asked from self-study contents.

Laboratory Work:
Laboratory work will be based on the above syllabus with a minimum of 10 experiments to be incorporated.

Suggested Readings/References:

1. Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, Springer
2. Naveed A. Sherwani, Algorithms for Vlsi Physical Design Automation, Kluwer Academic Publishers
3. Sadiq M Sait, Habib Youssef, VLSI Physical Design Automation: Theory and Practice, World Scientific
4. Andrew B Kahng, Jens Lienig, VLSI Physical Design: From Graph partitioning to Timing Closure, Springer

Details of Laboratory
Suggested List of Experiments

Sr. No.	Practical	No of Hours
1.	Physical design flow for semiconductor technology	02
2.	Routing optimization using shortest path graph theory	02
3.	Develop partitioning algorithm using programming language	02
4.	Develop placement algorithm using programming language	02
5.	Develop floorplanning algorithm using programming language	02
6.	Develop routing algorithm using programming language	02
7.	Perform Floorplanning on an IP through EDA tools	02
8.	Perform placement on IP through EDA tools	02
9.	Develop and optimize layout of an IP using EDA tool	02
10.	Perform routing on an IP using EDA tools	02
11.	Create, generate and analyse various physical design file formats	02
12.	Perform complete physical design flow for design-1	02
13.	Perform complete physical design flow for design-2	02
14.	Apply physical design algorithms on an IP	02
15.	Carry out timing analysis of IP	02