NIRMA UNIVERSITY

Institute:	Institute of Technology
Name of Programme:	MTech Semiconductor Technology
Course Code:	6EC351CC24
Course Title:	Semiconductor Assembly, Packaging and Testing
Course Type:	Core
Year of Introduction:	2024-25

L	T	Practical component				C
		LPW	PW	W	S	
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Course Learning Outcomes (CLOs)

At the end of the course, students will be able to

1. acquire fundamental knowledge of semiconductor packaging styles and materials (BL3)
2. apply test methods on semiconductor packaging. (BL5)
3. carry out failure mode analysis and assure the quality checks (BL5)
4. operate instruments and EDA tools required for semiconductor technology assembly, packaging and test. (BL6)

	Contents	Teaching hours (Total 45)
Unit I	**Semiconductor Packaging** Introduction to Assembly Flow, Packaging History, Package Families, Need of Packaging for Technologies.	**03**
Unit II	**Package Manufacturing Processes** Packaging Assembly Technology, Wafer Thinning, Dicing, Die Attach, Wire bonding, Flip Chip process, Flux Cleaning, Underfill, Encapsulation, Laser Marking, Solder Ball Attach, Reflow, Singulation, IC Packaging Toolsets & equipment operation, clean room operations.	**09**
Unit III	**Materials used in Semiconductor Packaging** Die Attached Adhesive, Underfill Materials, Bonding wires, Wafer Bumping, Under-bump Metallurgy, Ceramics and Glasses.	**06**
Unit IV	**Semiconductor Component and Package Test** Overview of Testing methodologies, components tested & their characteristics, Challenges in testing, Types of Testers (Automated test Equipment & Benchtop Testers), Components & Subsystems of Testers, Principles of Functional Testing, Parametric/ Boundary Scan /In-Circuit Test/ Flying Probe Test, Test Data Analysis, Design for Testability & Tester Calibration & Maintenance.	**10**
Unit V	**Electrical and Physical Failure Analysis** Package Failure Modes, Failure Detection Mechanisms, Failure Analysis Tools, Test Programs Debugging, Data Analytics, ESD & EMI Management.	**08**
Unit VI	**Quality and Statistical Process Control** Quality Control Plan (QCP) & Quality Management System (QMS), Incoming Material Inspection, In-Line Quality, Measurement System Analysis, Statistical analysis methods, Statistical Process Control (SPC), Fault Detection Control (FDC), Run-to-Run Control (R2R), Auto Defect	**05**

	Classification (ADC), Data Analytics, Machine Communication Protocol and System Integration.	
Unit VII	**Trends and Challenges** Advanced Packaging, Future Interconnect and Dielectric Materials, Future Packaging Options	**04**

Self Study:
The self-study contents will be declared at the commencement of the semester. Around 10% of the questions will be asked from self-study content.

Laboratory Work:
Laboratory work will be based on the above syllabus with a minimum of 10 experiments to be incorporated.

Suggested Readings/References:

1. John H. Lau, Semiconductor Advanced Packaging, Springer Santosh K. Kurinec, Krzysztof Iniewski, Nanoscale Semiconductor Memories: Technology and Applications, CRC Press
2. William Greig, Integrated Circuit Packaging, Assembly and Interconnections, Springer
3. Andrea Chen, Randy Hsiao-Yu Lo, Semiconductor Packaging, CRC press

Details of Laboratory
Suggested List of Experiments

Sr. No.	Practical	No of Hours
1.	To learn the complete assembly flow.	02
2.	To perform cleaning and thinning processes on wafer.	02
3.	To learn flip-chip process.	02
4.	To learn the characteristics and uses of materials used in semiconductor packaging.	02
5.	To perform marking using LASER.	02
6.	To perform encapsulation and singulation processes.	02
7.	To perform test methods on IC -1(Parametric Test).	02
8.	To perform test methods on IC -2 (Hot and Cold Tests).	02
9.	To perform test methods on IC(ATPG).	02
10.	To perform quality checks on IC.	02