NIRMA UNIVERSITY

Institute:	Institute of Technology
Name of Programme:	MTech Semiconductor Technology
Course Code:	6EC363CC24
Course Title:	Integrated Circuit Verification and Validation
Course Type:	Departmental Elective
Year of Introduction:	2024-25

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Course Learning Outcomes (CLOs)

At the end of the course, students will be able to

1. comprehend to Integrated Circuit validation process. (BL2)
2. perform the functional and timing verification on Integrated circuits. (BL3)
3. carry out the code coverage analysis. (BL4)
4. generation of test set to detect the faults in Integrated Circuits. (BL5)

	Contents	**Teaching hours (Total 45)**
Unit I	**Fundamentals of Verification** Introduction to verification, importance, complexity, methods to reduced verification efforts, verification at design abstraction levels.	**05**
Unit II	**Verification of Integrated Circuits** **V**erification flow, testbench architectures, testbench development for integrated circuits.	**05**
Unit III	**Verification Methods** Simulation and emulation-based verification, functional verification approaches, formal verification methods.	**05**
Unit IV	**Static Timing Analysis** Need of timing analysis, static timing analysis, dynamic timing analysis, critical path and maximum operating frequency, set-up and hold time violation, remedies for set-up and hold time violation	**10**
Unit V	**Coverage Analysis** significance of coverage, difference between code and functional coverage, code coverage: statement coverage, branch coverage, FSM coverage, toggle coverage.	**05**

Unit VI	**Validation** Introduction to validation, need of validation, standard techniques for validation and compliances, special mechanisms for SoC validation.	**10**
Unit VII	**Integrated Circuit Testing** Need of testing, fault modeling, Automatic Test Pattern Generation: test generation methods and algorithms.	**05**

Self Study:

The self-study contents will be declared at the commencement of the semester. Around 10% of the questions will be asked from self-study content.

Suggested Readings/References:

1. Janick Bergeron, Writing Testbenches-Functional Verification of HDL Models, Springer
2. M. L. Bushnell and V. D. Agrawal-Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits, Kluwer
3. Abramovici, M. A. Breuer and A. D. Friedman, Digital Systems Testing and Testable Design, Wiley/IEEE Press