NIRMA UNIVERSITY

Institute:	Institute of Technology
Name of Programme:	BTech (Electronics & Communication Engineering)
Course Code:	3EC503CC24
Course Title:	Computer Architecture
Course Type:	Core
Year of Introduction:	2024-25

L	T	Practical component				C
		LPW	PW	W	S	
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Course Learning Outcomes (CLOs)

At the end of the course, the students will be able to

1. demonstrate cache mapping and virtual memory address translation schemes (BL2)
2. analyse the performance of single and multicycle data path (BL4)
3. evaluate the performance of the processor for given specifications (BL5)
4. design an arithmetic logic unit for a given instruction set. (BL6)

	Contents	Teaching hours (Total 45)
Unit I	**Computer Performance:** Cost and performance, performance enhancement, Amdahl's law, performance estimation	**04**
Unit II	**Instruction Set Architecture of MIPS Processor:** Instruction format, instruction set, addressing modes, procedure and data, assembly language programming, instruction set variation	**06**
Unit III	**Arithmetic and Logical Unit (ALU) Design:** Design of adders and simple ALU, multiplier and divider	**06**
Unit IV	**Data Path and Control Path of MIPS Processor:** Instruction execution steps, single cycle and multi-cycle data path, performance of single and multi-cycle data path, control unit synthesis, microprogramming, pipe-lined data path, pipeline performance limits, data and control dependencies, branch prediction algorithms	**15**
Unit V	**Buses, Link and Interfacing:** Intra and intersystem links, types of buses and their characteristics, bus communication protocols, bus arbitration and performance, basic of interfacing and interfacing standards	**08**
Unit VI	**Memory Organisation:** Memory hierarchy, SRAM, DRAM, cache organisation, cache mapping schemes, improving cache performance, virtual memory, flash memory, address translation, translation look aside buffer	**06**

Self Study:

The self-study contents will be declared at the commencement of the semester. Around 10% of the questions will be asked from self-study content.

Laboratory Work:

Laboratory work will be based on the above syllabus with a minimum of 10 experiments to be incorporated.

Suggested Readings/References:

1. Behrooz Parahami, Computer Architecture from Microprocessor to Super Computer, Oxford university press
2. Govind Rajalu, Computer Architecture, Tata McGraw-Hill
3. D.Patterson and J. Hennessy, Computer Organisation and Design: The Hardware/Software Interface, Morgan Kaufman
4. Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Pearson Education

Details of Laboratory

Suggested List of Experiments

Sr. No.	Practical	No. of Hours
1.	Introduction to Computer Organisation and Architecture Simulator (COAS)	02
2.	Realise arithmetic and logical operations using COAS	04
3.	Design a combinational multiplier using COAS	02
4.	Implement shift-add algorithm for multiplication using Verilog HDL	02
5.	Implement shift-subtract algorithm for division using Verilog HDL	02
6.	Design and realise an n-bit barrel shifter using Generate a statement in Verilog HDL	02
7.	Design dual-port RAM using Verilog HDL which allows writing at only one port at the positive edge the clock	02
8.	Design & implement Memory Blocks using Verilog HDL & Mega Wizard Plug-In Manager	04
9.	Analysis of direct cache mapping scheme using COAS	02
10.	Analysis of set associative cache mapping scheme COAS	02
11.	Realise next address logic block for MiniMIPS instruction set	02
12.	Design and implement a control section for a single-cycle data path using Verilog HDL	02
13.	Design and implement a control section for the multi-cycle data path using Verilog HDL	04
14.	Implement a microprogrammed control unit for given instruction sets	02
15.	Design of Execution block of Microprocessor for predefined instruction set and write a test bench to verify it	04