NIRMA UNIVERSITY

Institute:	Institute of Technology
Name of Programme:	BTech Electronics & Communication Engineering
Course Code:	3EC605ME24
Course Title:	Testing and Verification of Digital Circuits
Course Type:	Departmental Elective
Year of Introduction:	2024-25

L	T	Practical component				C
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Course Learning Outcomes (CLOs)

At the end of the course, the students will be able to

1. develop the testbench for the functional verification of digital circuits (BL3)
2. analyse the digital circuits for static timing (BL3)
3. apply the test vector generation algorithm for logical faults (BL4)
4. design the scan chain insertion for synchronous circuits. (BL6)

	Contents	Teaching hours (Total 45)
Unit I	**Verification:** Importance of verification, verification plan, verification flow, verification environment, functional verification, testbench architecture, layered testbench, test bench development using verilog HDL, formal verification methods, code and functional coverages	07
Unit II	**Verification Language:** Need of verification language, concept of class, SystemVerilog: data types, randomisation, interface, modport, mailbox, development of testbench component using SystemVerilog	06
Unit III	**Static Timing Analysis:** Need of timing analysis, dynamic timing analysis, static timing analysis, critical path and maximum operating frequency, set-up and hold time violation, remedies for violation, time borrowing	05
Unit IV	**Introduction to Testing:** Testing philosophy, role of testing, digital and analog circuit testing, technology trends affecting testing, test economics, defining cost, benefit-cost analysis, the rule of ten, yield	03
Unit V	**Fault Modeling:** Defects-errors-faults, functional versus structural testing, level of fault models, a glossary of fault models, single stuck at fault, multiple stuck at faults, fault equivalence	05
Unit VI	**Automatic Test Pattern Generation (ATPG):** Digital circuit testing, testability measures: controllability, observability, basic and advanced combinational ATPG algorithms	06
Unit VII	**Design for Testability:** Ad-hoc DFT techniques, structured DFT, scan-chain insertion, scan architecture, test for scan circuits, full serial integrated scan, multiple scans, partial scan, isolated serial scan, non-isolated scan	06
Unit VIII	**Built in Self Test (BIST):** Introduction to BIST concepts, hardcore, level of test, test pattern generation for BIST, generic off line BIST architectures	04
Unit IX	**Board Level Test:** Introduction to boundary scan standards, JTAG 1149.1 architecture, TAP/TAM controller, boundary cell, types of modes	03

Self Study:
The self-study contents will be declared at the commencement of the semester. Around 10% of the questions will be asked from self-study content.

Laboratory Work:
Laboratory work will be based on the above syllabus with a minimum of 10 experiments to be incorporated.

Suggested Readings/References:

1. Janick Bergeron, Writing Testbenches-Functional Verification of HDL Models, Springer
2. M. L. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed -Signal VLSI Circuits, Kluwer
3. Abramovici, M. A. Breuer and A. D. Friedman, Digital Systems Testing and Testable Design, Wiley/IEEE Press
4. Laung-Terng Wang, VLSI Test Principles and Architecture, Morgan Kaufman.

Details of Laboratory
Suggested List of Experiments

Sr. No.	Practical	No. of Hours
1.	Functional verification of combinational digital design through the development of exhaustive linear Test bench	02
2.	Functional verification of sequential digital design through the development of exhaustive linear Test bench	02
3.	Development of layer test bench components for combinational circuit using System Verilog	04
4.	Development of layer test bench component for sequential circuit using System Verilog	04
5.	Formal Verification of digital design	02
6.	Code coverage analysis of test bench	02
7.	Functional coverage analysis of test bench	02
8.	Development of fault equivalence concept	02
9.	Development of testability concept	02
10.	Development of basic test generation algorithm	02
11.	Development of advanced test generation algorithm	04
12.	Automatic Test Pattern Generation (ATPG) for a given digital circuit using tool	02
13.	Design for Testability: multiplexer-based scan chain insertion for a given digital circuit	02
14.	Design for Testability: dual clock-based scan chain insertion for a given digital circuit	02
15.	JTAG boundary scan insertion	02