NIRMA UNIVERSITY
SCHOOL OF TECHNOLOGY, INSTITUTE OF TECHNOLOGY
M. Tech. in Electronics & Communication Engineering (VLSI Design)
M.Tech Semester - I

L	T	Practical component				C
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Course Code	**6EC104CC22**
Course Title	**Advanced Digital System Design using Programmable Logic**

Course Learning Outcomes (CLOs):

At the end of the course, students will be able to -

1. Implement the design from specification to net list level using hardware description language
2. Implement the digital designs on FPGA in context of synthesis, device utilization and speed and power optimization
3. Optimize the design using the concepts of simulation, synthesis and Place & Route

Syllabus: **Teaching Hours: 45**

UNIT I: **03**
Review of basic digital-logic design, Combinational logic, Structured logic implementation, Sequential logic, Finite-state machines

UNIT II: **06**
Overview of digital technology, Logic families, Interfacing, glue logic, RAM/ROM, Basic Programmable devices (PROMs , PALs and PLDs)

UNIT III: **06**
Synchronous circuits, FSM design, Algorithum state machine charts, Design example of sequential synchronous circuits, Asynchronous behaviour, analysis and synthesis of asynchronous circuits, Design examples

UNIT IV: **10**
Concepts of Verilog HDL for Behavioral, RTL, Data-flow, Structural and switch level Modeling

UNIT V: **10**
Computer-aided design, Logic compilation, Two-level and multi-level logic synthesis, Technology-independent optimization, Technology mapping, Sequential-logic synthesis, Tools for mapping to PLDs and FPGAs

UNIT VI: **10**
Programmable Logic Devices, CPLD and FPGA, Architectures and Technology, Realization of Digital Design on FPGA, Advances in FPGA

Self Study:
The self-study contents will be declared at the commencement of semester. Around 10% of the questions will be asked from self-study contents

Laboratory Work:
Laboratory work will be based on above syllabus with minimum 10 experiments to be incorporated.

Suggested Readings:

1. Brown Vranesic, Fundamentals of Digital Logic with Verilog Design. Tata McGrawHill
2. Wyane Wolf, FPGA Based System Design, Pearson
3. Sameer Palnitkar, Verilog HDL, Pearson