NIRMA UNIVERSITY
SCHOOL OF TECHNOLOGY, INSTITUTE OF TECHNOLOGY
M.Tech. in Electronics & Communication Engineering (VLSI Design)
M.Tech. Semester - II

L	T	Practical component				C
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Course Code	**6EC151CC22**
Course Title	**VLSI Design Verification and Testing**

Course Learning Outcomes (CLOs):

At the end of the course, students will be able to -

1. Apply the concepts of testing to improve the quality and yield of IC.
2. Develop the test bench for given behavioral and RTL design.
3. Develop the test set for given circuit using various test generation methods for digital circuits.
4. Identify the Design-for-Testability and Built-In-Self-Test methods for combinational and sequential CMOS circuits.

Syllabus: **Teaching Hours: 45**

UNIT I: Introduction **03**
Need of Testing, Different Roles of Testing, Cost and Yield considerations with reference to Testing

UNIT II: Functional Verification Methods and Tools **08**
Concept, test bench architecture, Verification Language, Simulation tools, Functional and Code Coverage

UNIT III: Formal Verification Methods **04**
Binary Decision Diagram, Equivalence Checking, Assertion based verification, Emulation

UNIT IV: Fault Models **10**
Stuck-at Models, Transistor Short-Open Model, Bridge Fault Models, Single-Stuck-At Models, Fault Equivalence and Fault Dominance

UNIT V: Automatic Test Pattern Generator **10**
Deterministic Test Pattern generation, Basic and Advance Algorithm for test pattern Generation, Types of test pattern sets, ATPG System

UNIT VI: Design-For-Test and Built-In-Self-Test **10**
Introduction, Testability Analysis, Adhoc DFT Methods, Structured DFT Methods, Scan-Chain Based Design, Built-In-Self-Test Design Rules, Logic BIST Architecture

Self-Study:
The self-study contents will be declared at the commencement of Semester. Around 10% of the questions will be asked from self-study contents.

Laboratory Work:
Laboratory work will be based on above syllabus with minimum 10 experiments to be incorporated.

Suggested Readings:

1. M. L. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits, Kluwer Academic Publishers
2. M. Abramovici, M. A. Breuer and A. D. Friedman, Digital Systems Testing and Testable Design, IEEE Press
3. Spear, Chris, Tumbush, Greg, System Verilog for Verification-A Guide to Learning the Testbench Language Features, Springer