NIRMA UNIVERSITY
SCHOOL OF TECHNOLOGY, INSTITUTE OF TECHNOLOGY
M.Tech. in Electronics & Communication Engineering (VLSI Design)
M.Tech. Semester - II
Department Elective I

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Course Code	**6EC161ME22**
Course Title	**VLSI Signal Processing**

Course Learning Outcomes (CLOs):

At the end of the course, students will be able to -

1. Estimate the iteration bound of given digital systems using data flow graph representation.
2. Apply pipelining and parallel processing to improve speed and power performance of the digital systems.
3. Perform folding, unfolding and retiming operations on the given digital systems.
4. Design digital processing systems architecture for performance improvement in terms of area, power and speed.

Syllabus: **Teaching Hours:45**

UNIT I: Introduction to DSP Systems **06**

Typical DSP algorithms, Representation of DSP Algorithms, Data Flow Graph Representations, Loop Bound and Iteration Bound, Algorithms for Computing iteration Bound.

UNIT II: Pipelined and Parallel Processing **04**

Pipelining of FIR Filters, Parallel Processing, Pipelining and Parallel Processing for Low Power

UNIT III: Retiming, Folding and Unfolding **11**

Parallel FIR Filters, Retiming of DSP Systems, Data Flow Graph Algorithms for retiming Definitions Properties, Retiming Techniques, Algorithms for Unfolding, Folding Transformations, Folding of Multirate Systems

UNIT IV: Systolic Architecture and Filter Structures **08**

Applications Systolic, Systolic Array Design, FIR Systolic Arrays, Matrix Multiplication and 2D Systolic Array Design, Digital Basic Lattice Structure and Schur Algorithm, Pipelining of Lattice IIR Digital Filters, Low power CMOS Lattice IIR Filters.

UNIT V: Fast Convolution **05**

Cook - Toom Algorithm, Winograd Algorithm, Iterated Algorithm, Cyclic Convolution, Design of fast convolution Algorithm.

UNIT VI: Bit Level Arithmetic Architectures **05**

Parallel Multipliers, Bit Serial Multipliers, Bit Serial Filter Design and Implementation, Canonic Signed Digit Arithmetic, Distributed Arithmetic

UNIT VII: Synchronous, Wave, Asynchronous Pipelines and Low Power Design **06**

Synchronous Pipelining and Clocking Styles, Clock Skew and Clock Distribution in Bit Level Pipelined VLSI Designs, Wave Pipelining, Asynchronous Pipe-lining, Scaling versus Power Consumption, Power Reduction Techniques, Power Estimation Approaches.

Self-Study:

The self-study contents will be declared at the commencement of Semester. Around 10% of the questions will be asked from self-study contents.

Suggested Readings:

1. VLSI Digital Signal Processing systems, Design and Implementation by Keshab K.Parthi, Wiley, Inter Science
2. Digital Signal Processing with FPGA by Uwe, Meyer-Bease, 3rd Springer