NIRMA UNIVERSITY
SCHOOL OF TECHNOLOGY, INSTITUTE OF TECHNOLOGY
M.Tech. in Electronics & Communication Engineering (VLSI Design)
M.Tech. Semester - II
Department Elective I

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Course Code	**6EC162ME22**
Course Title	**Low Power VLSI Design**

Course Learning Outcomes (CLOs):

At the end of the course, the students will be able to -

1. Analyze the static and dynamic power dissipation for CMOS digital designs.
2. Estimate power dissipation at different abstraction levels using simulation and probability techniques.
3. Apply low power schemes at architecture and circuit level.

Syllabus: **Teaching Hours: 45**

UNIT I: Need for Low Power VLSI Chips **08**

Charging and discharging of capacitance, short circuit currents in CMOS circuit, CMOS leakage current, Static current, Basic Principles of low power Design, low power figure of merit

UNIT II: Power Analysis **08**

Simulating at various abstraction level like circuit, gate, architecture level for power estimation, UPF (unified power format), Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy

UNIT III: Low Power Design at Circuit and Logic Level **12**

Transistor and gate sizing, equivalent pin ordering, Network restructuring and reorganizing, Special latches and flip flop, low power digital cell library, Adjustable device threshold voltage, Gate reorganization, signal gating, logic encoding, state machine encoding, Pre computation logic

UNIT IV: Special Techniques **03**

Power reduction in clock network, CMOS floating node, low power bus, Delay balancing, low power techniques for SRAM

UNIT V: Low power Architecture and Systems **05**

Power performance Management, Switching activity reduction, Parallel architecture for voltage reduction

UNIT VI: Advance Techniques for Power Reduction **04**

Adiabatic computation, Pass transistor logic synthesis, Asynchronous **circuits**

UNIT VII: Low Power Testing **05**

Introduction, sources of excessive Power dissipation during testing, power dissipation estimation, test power optimization.

Self-Study:

The self-study contents will be declared at the commencement of Semester. Around 10% of the questions will be asked from self-study contents.

Suggested Readings:

1. Gary K. Yeap, Practical Low Power Digital VLSI Design, Kluwer
2. Rabaey, Pedram, Low Power Design Methodologies, Kluwer
3. Kaushik Roy, Sharat Prasad, Low-Power CMOS VLSI Circuit Design, Wiley
4. Kint-Seng and Kaushik Roy, Low Voltage Power VLSI Subsystems, TM
5. Anantha Chandrakasan, Low Power CMOS Design, IEEE Press