

**NIRMA UNIVERSITY**  
**SCHOOL OF TECHNOLOGY, INSTITUTE OF TECHNOLOGY**  
**M.Tech. in Electronics & Communication Engineering (VLSI Design)**  
**M.Tech. Semester - II**  
**Department Elective II**

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<b>Course Code</b>	<b>6EC168ME22</b>
<b>Course Title</b>	<b>Deep SubMicron CMOS IC</b>

**Course Learning Outcomes (CLOs):**

At the end of the course, students will be able to -

1. Design the small scale MOS digital circuits and cells for given specifications.
2. Apply scaling methods to digital logic design and determine performance parameters.
3. Design deep submicron CMOS logic using lambda rule.

**Syllabus:**

**Teaching Hours:45**

**UNIT I: Impact of Scaling**

**10**

Deep Sub-micron MOS Transistor Theory & impact of device scaling, Deep Sub-micron Transistor Models, Subthreshold current and subthreshold swing, Drain Induced Barrier Lowering (DIBL), Punch through, Gate Induced Drain Leakage (GIDL), Deep Sub-micron Noise & Noise Tolerant Designs, Crosstalk, Leakage, Supply Noise & Process Variations, Noise Tolerant

**UNIT II: Circuit Design Styles**

**10**

(skewed CMOS, noise tolerant domino, layout styles for high noise immunity) CMOS Deep Submicron Fabrication Technology, Silicon Processing Technology Steps ( n-Well CMOS Technology, p-Well, Twin Tub, and Triple Well Technologies), Deep submicron

**UNIT III: Fabrication Technology**

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Trench Isolation, Antenna Rules, CMP Rules, Design Margin, Supply Voltage, Temperature, Process Variation, Design Corners, Matching,

**UNIT IV: Delay Tracking**

**05**

Latch up and Reliability (Electromigration, Electrostatic discharge (ESD), Electrical overstress (EOS), Self-heating, Hot Carriers), Latchup, Latchup Prevention, Overvoltage, Time-Dependent Dielectric Breakdown (TDDB)

**UNIT V: Testing for DSM VLSI Design**

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S chmoo Plots, Automatic Test Equipment, Additional JTAG Instructions, Iddq testing of circuits with high intrinsic leakage: delta Iddq, two parameter tests. Idd waveform analysis

**Self-Study:**

The self-study contents will be declared at the commencement of Semester. Around 10% of the questions will be asked from self-study contents.

**Suggested Readings:**

1. Harry Veendric, Deep Sub micron CMOS ICs, Springer
2. Christian Piguët, Low power Electronics Design, Chemical Rubber Company Press