NIRMA UNIVERSITY
SCHOOL OF TECHNOLOGY, INSTITUTE OF TECHNOLOGY
M.Tech. in Electronics & Communication Engineering (VLSI Design)
M.Tech. Semester - II
Department Elective II

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Course Code	**6EC169ME22**
Course Title	**VLSI System on Chip**

Course Learning Outcomes (CLOs):

At the end of the course, students will be able to -

1. Analyze modeling styles for design of system on chip.
2. Design data path architectures and solve intra-chip communication issues for given system on chip.
3. Apply partitioning and floor planning algorithms for effective system on chip design.
4. Utilize System Verilog, TLM, and System C for modeling and testing of system on chip.

Syllabus: **Teaching Hours:45**

UNIT I: Introduction **05**
System on Chip technology challenges, System on a Chip (SoC) components, SoC design methodology.

UNIT II: SoC Architecture **07**
Parameterized SoC, SoC peripheral cores, SoC and Interconnect Centric Architectures

UNIT III: System Level Design **09**
System level design representations and modelling languages, Target architecture models, Intra-chip communication, Graph partitioning algorithms, Floor planning algorithms, Task time measurement

UNIT IV: Synthesis and Timing Analysis **09**
Interconnect latency modelling, Back annotation of lower level timing to high-level models, Synthesis of SoC components.

UNIT V: SoC Verification and Testing **15**
System level verification, Block level verification and Hardware/Software Co-verification using System C, TLM, System Verilog, Emulation, Physical Verification.

Self-Study:
The self-study contents will be declared at the commencement of Semester. Around 10% of the questions will be asked from self-study contents.

Suggested Readings:

1. Wayone Wolf, Modern VLSI Design: SOC Design, Pearson Education.
2. Prakash Rashnikar, Peter Paterson, Lenna Singh, System-on-a-Chip, Verification Methodology & Techniques, Kluwer Academic Publishers.
3. Alberto Sangiovanni Vincentelli, Surviving the SOC Revolution: A Guide to Platform based Design, Kluwer Academic Publishers.
4. J. Bhasker, A System C Primer, Star Galaxy.