# NIRMA UNIVERSITY SCHOOL OF TECHNOLOGY, INSTITUTE OF TECHNOLOGY M.Tech. in Electronics & Communication Engineering (VLSI Design) M.Tech. Semester - II

## **Department Elective III**

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<b>Course Code</b>	6EC170ME22
Course Title	Advanced Topics in Verification and System Verilog

### **Course Learning Outcomes (CLOs):**

At the end of the course, the students will be able to -

- 1. Use the concept of Object-Oriented Programming for verification
- 2. Develop the higher level testbench using System Verilog
- 3. Choose effective methods for verification of complex digital designs.

#### Syllabus: **Teaching Hours: 30** 04 **UNIT I: Timing Analysis** Importance, Issues and Challenges, Static and Dynamic Timing Analysis, Set-up and Hold Violation and Remedies 04 **UNIT II: Logic and Fault Simulation** Introduction, Simulation Methods, Logic Simulation, Fault Simulation, Serial and Parallel fault simulation **UNIT III: Higher Level Verification Guidelines** 06 Constrained Random Stimulus, Testbench Components, Layered Testbenches, Code Reuse **UNIT IV: Data Types, Procedural Statements and Routines** 05 Data Types, Types of Arrays, Packages, Tasks, Functions, Void Functions, Time Values, Case study **UNIT V: OOPS for Testbench** 06 OOPS Terminology, Class Methods, Building a testbench using OOPs **UNIT VI: Functional Coverage** 05 Gathering Coverage data, Coverage types, Functional Coverage Strategies, Anatomy of a cover group, Analyzing coverage data

## Self-Study:

The self-study contents will be declared at the commencement of Semester. Around 10% of the questions will be asked from self-study contents.

## Laboratory Work:

Laboratory work will be based on the above syllabus with a minimum of 10 experiments to be incorporated.

## **Suggested Readings:**

1. Jenick Bergeron, Writing Testbenches using System Verilog, Springer

2. Spear, Chris, Tumbush, Greg, System Verilog for Verification-A Guide to Learning the Testbench Language Features, Springer