NIRMA UNIVERSITY
SCHOOL OF TECHNOLOGY, INSTITUTE OF TECHNOLOGY
M. Tech. in Electronics & Communication Engineering (Embedded System)
M.Tech Semester - I

L	T	Practical component				C
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Course Code	6EC201CC22
Course Title	Advanced Digital System Design

Course Learning Outcomes (CLOs):

At the end of the course, students will be able to -

1. Design digital circuits and system using MSI & LSI logic.
2. Implement digital systems using finite state machine and state machine chart.
3. Analyze timing performance of digital systems.
4. Implement the digital systems on reconfigurable platform using hardware description language.

Syllabus: **Teaching Hours:45**

UNIT I: Introduction to Digital Systems Design **07**

overview of digital fundamentals, design with LSI and MSI Logics, Advanced Boolean algebra and advanced K Map for optimization, Hazards in combinational networks

UNIT II: Synchronous Sequential Logic **10**

Analysis and design of Synchronous sequential Finite State Machine, Optimization using state reduction and state assignment algorithms, Design of shift registers and Counters, HDL for Sequential Circuits, Timing and Triggering Consideration in FSM, Clock issues and design of synchronizer

UNIT III: Hardware Description Languages (Verilog) **10**

Fundamentals of Verilog, Overview of Digital Design with Verilog HDL, Hierarchical Modeling Concepts, Top-down and bottom-up design methodology, Modules and Port, Gate-Level Modeling, Dataflow Modeling, Behavioral Modeling, Tasks and Functions, RTL Description of Simple Machine and Design from RTL description, Test Bench, Synthesis Issues

UNIT IV: Asynchronous Sequential Logic **05**

Analysis and design of asynchronous sequential circuits, primitive flow table, reduction of state and flow tables, concept of race, race free state assignment, critical race and essential hazards is asynchronous FSM

UNIT V: SM Charts and Microprogramming **05**

State machine charts, derivation of SM charts, realization of SM charts, Linked microprogramming, Hierarchical & Concurrent FSM (HCFSM).

UNIT VI: Programmable Logic Devices **03**

Introduction to PLDs, PROM based design, PAL and PLA Architectures, Sequential PAL, Design of PLD's using HDL

UNIT VII: FPGA & CPLD Architectures **05**

Classification of FPGs, Architecture of CPLD and FPGA, Architecture of configurable block, Input/output Blocks, programmable Interconnect, Study of Xilinx , Altera FPGAs

Self Study:

The self-study contents will be declared at the commencement of semester. Around 10% of the questions will be asked from self-study contents.

Laboratory Work:
Laboratory work will be based on above syllabus with minimum 10 experiments to be incorporated.

Suggested Readings:

1. Charles H Roth Jr. and Lizy Kurian John, and Byeong Kill Lee, "Digital Systems Design using VerilogHDL", Cengage Learning India.
2. Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Second Edition, Prentice Hall PTR.
3. Charles H.Roth, Jr. "Fundamentals of Logic Design", Jaico Publishing
4. Michael D. Ciletti, Advanced Digital Design with the Verilog HDL, PHI
5. Joseph Cavanagh, Digital Design and Verilog HDL Fundamentals, CRC Press
6. Chan and Mourad, Digital Design using Field Programmable Gate Arrays, Prentice Hall of India
7. William I. Fletcher, An Engineering Approach to Digital Design, Prentice Hall of India
8. J. Bhaskar, Verilog HDL Synthesis: A Practical Primer, Star Galaxy Publishing.
9. Pong P. Chu, FPGA Prototyping by Verilog Examples, Wiley.