NIRMA UNIVERSITY

Institute:	**Institute of Technology, School of Technology**
Name of Programme:	**B.Tech. in Electronics & Communication Engineering**
Course Code:	4EC502ME25
Course Title:	**Modern Processor Architecture**
Course Type:	**Department Elective**
Year of Introduction:	**2025-26**

L	T	Practical Component				C
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Course Learning Outcomes (CLOs):

At the end of the course, the students will be able to

1 comprehend the design steps for pipelined processors and classify pipelined processors (BL2)
2 deploy suitable superscalar technique(s) to enhance the performance of processors for given specifications (BL3)
3 recommend suitable data and memory flow techniques to overcome hazards in modern processor architectures (BL4)
4 design finite state machine diagram to overcome cache coherence issues in the multiprocessor system. (BL6)

Unit	Contents	Teaching hours (Total 45)
Unit I	**Processor Design:** Introduction and evolution, Instruction set processor design, Principles of processor performance, Instruction level parallel processing	**04**
Unit II	**Pipelined Processors and Super Scalar Organization:** Pipelining fundamentals, Pipelined processor design, Deeply pipelined processors, Limitations of Scalar pipelines, Superscalar pipeline overview	**10**
Unit III	**Memory and I/O Systems:** Introduction and concept of latency and bandwidth, Memory hierarchy implementation, Virtual Memory systems, Input/output systems	**04**
Unit IV	**Super Scalar Techniques:** Instruction Flow techniques, Register Data Flow Techniques, Memory data flow Techniques	**13**
Unit V	**Multiprocessors and Thread-Level Parallelism:** Introduction to Multiprocessor Systems, Symmetric Shared-Memory Architectures, Performance of Symmetric Shared-Memory Multiprocessors, Distributed Shared Memory and Directory-Based Coherence, Explicitly, multithreaded processors	**08**
Unit VI	**Case Studies:** Recent Modern Processor Architectures, RISC-V Architectures	**06**

Self Study:
The self-study contents will be declared at the commencement of the semester. Around 10% of the question will be asked from self-study contents.

Tutorial Work: This shall consist of at least 10 tutorials based on the above syllabus.

Suggested Readings/ Reference:

1. J. Shen and M. Lipasti, *Modern processor Design Fundamentals of Superscalar Processors*, Tata McGraw-Hill
2. D. Patterson and J. Hennessy, *Computer Organization and Design: The Hardware/Software Interface*, Morgan Kaufman
3. William Stallings, *Computer Organization & Architecture Designing for Performance*, Pearson
4. Behrooz Parahami, *Computer Architecture from Microprocessor to Super Computer*, Oxford

Suggested List of Tutorials

Sr. No.	Name of Experiments/Exercises	Hours
1.	General Purpose Processor Performance Measurement	01
2.	Study of Benchmarks	01
3.	Design of Pipelined Processors	01
4.	Performance measurement of Pipelined Processors	01
5.	Study of Simulators for Processor Architecture evaluation	01
6.	Memory Hierarchy	01
7.	Virtual Memory Management System	01
8.	Processor I/O Systems	01
9.	Super Scalar Architecture: Instruction Flow techniques	01
10.	Super Scalar Architecture: Register Data Flow Techniques	01
11.	Super Scalar Architecture: Memory data flow Techniques	01
12.	Graphics Processor Architecture	01
13.	Instruction Level Parallelism	01
14.	Thread Level Parallelism	01
15.	Message Passing Interface and Programming	01