Nirma University
School of Technology, Institute of Technology
B. Tech (Instrumentation and Control Engineering)

Semester VII

L	T	P	C
3	0	0	3

Course Code	**2ICDE08**
Course Title	**VLSI Design**

Course Outcomes (CO):

At the end of the course, students will be able to -

1. analyze the different digital VLSI circuits
2. model the CMOS circuit with equivalent parameters
3. design combinational, sequential and dynamic logic circuits using CMOS for given specifications.
4. develop various types of memory circuits

Syllabus: **Teaching Hours**

UNIT 1 : Introduction of VLSI **02**

Historical perspective, Objective and organization, Overview of VLSI Design Methodologies, VLSI design flow, Design Hierarchy, Concept of Regularity, Modularity and Locality, VLSI design Styles, Design Quality, Packaging Technology.

UNIT 2: MOS Basics Scaling and Effects of Scaling on MOS **05**

MOSFET Basics, V-I Characteristics, MOSFET scaling, Small-geometry effects, MOSFET capacitances

UNIT 3: MOS Inverter Static Characteristics **08**

Introduction, Resistive load Inverter, Inverter with n-type MOSFET load (Enhancement & Depletion type MOSFET load), CMOS Inverter.

UNIT 4: MOS Inverters Switching Characteristics and Interconnect Effects **07**

Introduction, Delay-time definitions, Calculation of Delay times, Inverter design with delay constraints, Estimation of Interconnect Parasitic, Calculation of interconnect delay, Switching Power Dissipation of CMOS Inverters.

UNIT 5: Combinational MOS Logic Circuits **05**

Introduction, MOS logic circuits with Depletion NMOS Loads, CMOS logic circuits, Complex logic circuits, CMOS Transmission Gates (TGs).

UNIT 6: Sequential MOS Logic Circuits **03**

Introduction, Behaviour of Bistable elements, SR latch circuit, Clocked latch & Flip-flop circuits, CMOS D-latch & Edge-triggered flip-flop.

UNIT 7: Dynamic Logic Circuits **05**

Introduction, Basic Principles of pass transistor circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, CMOS Dynamic Circuit Techniques.

UNIT 8: CMOS memory circuit **07**

Design of ROM, SRAM and DRAM cells. Sequential MOS Logic Design, Static and dynamic latches, flip flops & registers, CMOS Schmitt trigger, Monostable sequential and Astable circuits, adders and multiplier circuits

UNIT 9: Advances in VLSI Design **03**

Challenges with MOS, MOS Alternate Technologies, Low Power Technology

Self-Study:

The self-study content will be declared at the commencement of the semester. Around 10% of the question will be asked from self-study content.

References:

1. Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits – Analysis and Design, TATA McGraw-Hill
2. Pucknell and Eshraghian, Basic VLSI Design, PHI
3. Amar Mukerji, Introduction to nMOS and CMOS VLSI System Design, Prentice Hall
4. Neil H. E. Weste, David Money Harris, CMOS VLSI Design: A Circuits and Systems Perspective, Addison Wesley
5. J.M. Rabey , Digital Integrated Circuits Design, Pearson Education

L= Lecture, T= Tutorial, P= Practical, C = Credit