NIRMA UNIVERSITY

Institute:	Institute of Technology
Name of Programme:	B. Tech in Electronics and Instrumentation Engineering
Course Code:	2EIDE08
Course Title:	VLSI Design
Course Type:	([] Core/[] Value Added Course/[√] **Departmental Elective**/ [] Institute Elective/[]University Elective/[]Any other)
Year of introduction:	2023-2024

Credit Scheme

L	T	Practical component				C
		LPW	PW	W	S	
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Course Learning Outcomes (CLO):

At the end of the course, students will be able to –

1. analyze the different digital VLSI circuits
2. model the CMOS circuit with equivalent parameters
3. design combinational, sequential and dynamic logic circuits using CMOS for given specifications.
4. develop various types of memory circuits

Syllabus: **Total Teaching hours:45**

Unit	Syllabus	Teaching hours
Unit-I	**Introduction of VLSI** Historical perspective, Objective and organization, Overview of VLSI Design Methodologies, VLSI design flow, Design Hierarchy, Concept of Regularity, Modularity and Locality, VLSI design Styles, Design Quality, Packaging Technology	02
Unit-II	**MOS Basics Scaling and Effects of Scaling on MOS** MOSFET Basics, V-I Characteristics, MOSFET scaling, Small-geometry effects, MOSFET capacitances	05
Unit-III	**MOS Inverter Static Characteristics** Introduction, Resistive load Inverter, Inverter with n-type MOSFET load (Enhancement & Depletion type MOSFET load), CMOS Inverter.	08

Unit-IV	**MOS Inverters Switching Characteristics and Interconnect Effects** Introduction, Delay-time definitions, Calculation of Delay times, Inverter design with delay constraints, Estimation of Interconnect Parasitic, Calculation of interconnect delay, Switching Power Dissipation of CMOS Inverters.	07
Unit-V	**Combinational MOS Logic Circuits** Introduction, MOS logic circuits with Depletion NMOS Loads, CMOS logic circuits, Complex logic circuits, CMOS Transmission Gates (TGs).	05
Unit-VI	**Sequential MOS Logic Circuits** Introduction, Behaviour of Bistable elements, SR latch circuit, Clocked latch & Flip-flop circuits, CMOS D-latch & Edge-triggered flip-flop.	03
Unit -VII	**Dynamic Logic Circuits** Introduction, Basic Principles of pass transistor circuits, Voltage Bootstrapping, Synchronous Dynamic Circuit Techniques, CMOS Dynamic Circuit Techniques.	05
Unit-VIII	**CMOS memory circuit** Design of ROM, SRAM and DRAM cells. Sequential MOS Logic Design, Static and dynamic latches, flip flops & registers, CMOS Schmitt trigger, Monostable sequential and Astable circuits, adders and multiplier circuits	07
Unit-IX	**Advances in VLSI Design** Challenges with MOS, MOS Alternate Technologies, Low Power Technology	03

Self-Study: The self-study content will be declared at the commencement of the semester. Around 10% of the question will be asked from self-study content.

Suggested List of Experiments: -

Suggested Readings/ References:

1.Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits – Analysis and Design, TATA McGraw-Hill

2.Pucknell and Eshraghian, Basic VLSI Design, PHI

3. Amar Mukerji, Introduction to nMOS and CMOS VLSI System Design, Prentice Hall

4. Neil H. E. Weste, David Money Harris, CMOS VLSI Design: A Circuits and Systems Perspective, Addison Wesley

5. J.M. Rabey , Digital Integrated Circuits Design , Pearson Education

Suggested Case List: -