NIRMA UNIVERSITY

Institute:	Institute of Technology
Name of Programme:	B.Tech. in Electronics and Instrumentation Engineering
Semester:	V
Course Code:	3EI602ME24
Course Title:	Digital Signal Processing
Course Type:	Departmental Elective-I
Year of Introduction:	2024-25

L	T	Practical component				C
		LPW	PW	W	S	
3	-	2	-	-	-	4

Course Learning Outcomes (CLOs):

At the end of the course, the students will be able to –

1. understand direct Fourier transform and fast Fourier transform **(BL2)**
2. illustrate DSP processors **(BL2)**
3. design finite impulse response filters **(BL3)**
4. design infinite impulse response filters **(BL3)**
5. realize FIR and IIR filter structures **(BL4)**

Unit	Contents	Teaching hours (Total 45)
Unit-I	**Signal processing fundamentals** A/D, D/A conversion and Nyquist rate, frequency aliasing due to sampling, need for anti-aliasing filters, computational complexity of the DFT and the FFT, algorithmic development and computational advantages of the FFT, inverse FFT, implementation of the FFT.	**08**
Unit-II	**FIR filters** Ideal digital filters, realizability and filter specifications, classification of linear phase FIR filters, design using direct truncation, window methods and frequency sampling, least-squares optimal FIR filters, minimax optimal FIR filters, design of digital differentiators and Hilbert transformers, comparison of design methods.	**10**
Unit-III	**IIR filters** Design of analog prototype filters, analog frequency transformations, impulse invariance method and digital frequency transformations, bilinear transformation, analog prototype to digital transformations, difficulties in direct IIR filter design, comparisons with FIR filters	**10**
Unit-IV	**Filter realization** Structures for FIR filters, structures for IIR filters, state-space analysis and filter structures, fixed point and floating-point representation of numbers, errors resulting from rounding and truncating, quantization effects of filter coefficients, round-off effects of digital filters.	**10**
Unit-V	**DSP processors** Computer architectures for signal processing – Harvard architecture and pipelining, general purpose digital signal processors, selection of DSPs, implementation of DSP algorithms on a general-purpose DSP, special purpose hardware – hardware digital filters and hardware FFT processors, evaluation boards for real-time DSP.	**07**

Self Study:
The self-study contents will be declared at the commencement of semester. Around 10% of the questions will be asked from self study contents.

Laboratory Work:
This shall consist of at least 10 practicals based on the above syllabus.

Suggested Reading:

1. J. Proakis, D. Manolakis, Digital Signal Processing: Principles, Algorithms, & Applications, Prentice Hall of India
2. E. Ifeachor, B. Jervis, E. Dagless, J. O'Reilly, Digital Signal Processing: A Practical Approach, Pearson Education Asia
3. S.K. Mitra, Digital Signal Processing: A Computer-Based Approach, McGraw Hill
4. A. Anand Kumar, Digital Signal Processing, PHI publication
5. P.M. Embree, D. Danieli, D., C++ Algorithms for Digital Signal Processing, Prentice Hall

Suggested List of Experiments (not restricted to the following):
(Only for Information)

1.	Waveform generation.	**(02 Hrs)**
2.	To find the DFT and IDFT for the given input sequence.	**(02 Hrs)**
3.	Verification of Sampling Theorem	**(02 Hrs)**
4.	To find the FFT and IFFT for the given input sequence.	**(02 Hrs)**
5.	Generation of AM, FM, and PWM waveforms and their spectrum.	**(02 Hrs)**
6.	Design FIR filter using window method: Low pass filter.	**(02 Hrs)**
7.	Design FIR filter using window method: High pass filter.	**(02 Hrs)**
8.	Design FIR filter using window method: Band pass filter.	**(02 Hrs)**
9.	Design FIR filter using window method: Band stop filter.	**(02 Hrs)**
10.	Design IIR filter.	**(02 Hrs)**
11.	Generation of response of Low pass and High Pass Filters using DSP Trainer Kit	**(02 Hrs)**
12.	DC Motor 4- quadrant speed control using DSP.	**(02 Hrs)**

L = Lecture, T = Tutorial, P = Practical, C = Credit

w.e.f. the academic year 2024 - 25 and onwards