NIRMA UNIVERSITY

Institute:	**Institute of Technology, School of Technology**
Name of Programme:	**BTech in Electronics and Instrumentation Engineering**
Semester:	**VII**
Course Code:	4EI602ME25
Course Title:	**VLSI Design**
Course Type:	**Department Elective - IV**
Year of Introduction:	**2024-2025**

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Course Learning Outcomes (CLOs):

At the end of the course, the students will be able to –

1	parametric analysis of circuit families based on design and operation	(BL4)
2	utilize different digital modules with applications	(BL4)
3	analysis of FPGA architectures for desing and testing framework	(BL4)
4	testing strategies and methodology analysis with evaluation of parameters.	(BL5)

Unit	Contents	Teaching hours (Total 45)
Unit-I	**Introduction to MOS transistor** MOS Transistor, CMOS logic, Inverter, Pass Transistor, Transmission gate, Layout Design Rules, Gate Layouts, Stick Diagrams, Long-Channel I-V Charters tics, C-V Charters tics, non-ideal I-V Effects, DC Transfer characteristics, RC Delay Model, Elmore Delay, Linear Delay Model, Logical effort, Parasitic Delay, Delay in Logic Gate, Scaling.	09
Unit-II	**Combinational MOS logic circuits** Circuit Families: Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Pass Transistor Logic, Transmission Gates, Domino, Dual Rail Domino, CPL, DCVSPG, DPL, Circuit Pitfalls. Power: Dynamic Power, Static Power, Low Power Architecture.	08
Unit-III	**Sequential circuit design** Static latches and Registers, Dynamic latches and Registers, Pulse Registers, Sense Amplifier Based Register, Pipelining, Schmitt Trigger, Monostable Sequential Circuits, Astable Sequential Circuits. Timing Issues: Timing Classification of Digital System, Synchronous Design.	10

Unit-IV	**Design of arithmetic building blocks and subsystem** Arithmetic Building Blocks: Data Paths, Adders, Multipliers, Shifters, ALUs, power and speed tradeoffs, Case Study: Design as a tradeoff. Designing Memory and Array structures: Memory Architectures and Building Blocks, MemoryCore, Memory Peripheral Circuitry.	10
Unit-V	**Implementation strategies and testing** FPGA Building Block Architectures, FPGA Interconnect Routing Procedures. Design for Testability: Ad Hoc Testing, Scan Design, BIST, IDDQ Testing, Design for Manufacturability, Boundary Scan.	08

Self Study:
The self -study contents will be declared at the commencement of semester. Around 10% of the questions will be asked from self study contents.

Tutorial:
Tutorial work will be based on above syllabus with minimum 10 tutorials to be incorporated.

Suggested Readings/ References:

1. Neil H.E. Weste, David Money Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th Edition, Pearson , 2017 (UNIT I,II,V)
2. Jan M. Rabaey ,Anantha Chandrakasan, Borivoje. Nikolic, *Digital Integrated Circuits: A Design perspective*, Second Edition , Pearson , 2016.(UNIT III,IV)
3. M.J. Smith, *Application Specific Integrated Circuits*, Addisson Wesley, 1997
4. Sung-Mo kang, Yusuf leblebici, Chulwoo Kim. *CMOS Digital Integrated Circuits: Analysis & Design*, 4th edition McGraw Hill Education,2013
5. Wayne Wolf, *Modern VLSI Design: System On Chip*, Pearson Education, 2007
6. R.Jacob Baker, Harry W.LI., David E.Boyee, *CMOS Circuit Design, Layout and Simulation*, Prentice Hall of India 2005.

Suggested List of Tutorial :

Sr. No	Title
1.	Study related to the parameter analysis of MOS based circuits and different delay models
2.	Study related to the various design rules and diagrams with non-linear effects
3.	Study of various parameters related to the logic families and their different architectures
4.	Study and analysis of various power dissipation parameters along with different combinations
5.	Study and analysis of various sequential logic designs and their applications
6.	Study and analysis of various approaches and parameters related to the specific sequential circuits
7.	Study and analysis of various memory architectures and their applications
8.	Study and analysis of parameters trade-offs for arithmetic building blocks
9.	Analysis of various implementation strategies of FPGA
10.	Study of distinct testing methodologies for FPGA design